Fabrication and Characterization of Ion-Engineered III-V Matrix for Photonic Integrated Circuits



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This thesis, titled, "Fabrication and Characterization of Ion-Engineered III-V Matrix for Photonic Integrated Circuits", is submitted by Khurram Hussain, Registration No.: 62-FET/PhDEE/F13; to the Faculty of Engineering and Technology (FET), International Islamic University Islamabad (IIUI), in partial fulfillment of the requirements for the degree of Ph.D in Electronics Engineering.

The work presented in this thesis is carried out in the Centre For Advanced Electronics & Photovoltaic Engineering, International Islamic University Islamabad, Pakistan

This Thesis is

DEDICATED TO

My Teachers, My Mother and Family

CERTIFICATE OF APPROVAL

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Abstract

In our study we have extensively studied the two photonically active integrated circuit's platforms, namely GaN and InGaAsP's as they have now become a global contender for their wide range of optoelectronic and photonic applications. The GaN acts as a promising matrix; compatible with silicon and sapphire substrates. Both the carrier transport and carrier removal techniques are vital to develop the efficient platform for the integration of photonic circuits. We demonstrate the carrier removal mechanism in silicon (Si) doped GaN (0001) epitaxially grown on c-plane sapphire wafer using ion engineering of the devices. For that purpose, Helium (He⁺) and Carbon (C⁺) ions with pre-designed doses and energies are used to irradiate the device structures. We have modelled and fabricated ion-engineered regions within the active layers and studied the carrier transport properties on said regions to isolate that particular part with the active photonic components placed at the common platform. After ion irradiation, detailed analysis in terms of electric field dependent current characteristics, sheet resistance, carrier mobilities, activation energies, dark and photo currents under zero (ground) and multiple biases are examined to see the extent of charge leakage and to map the charge behavior under nominal operation. Device characteristics under wide regime of annealing temperatures ranging from 300°C to 1000°C are mapped to evaluate the thermal stability of implant driven isolated regions. Activation energies of implanted and parent regions have also been studied. The dark and photon driven electric currents at ground and under bias conditions have been measured to investigate the photoinduced transport phenomenon. For InGaAsP; We have provided an insight about the effective multi-implant ion-assisted carrier removal capability of the highly conductive epitaxially grown InGaAsP/InP device matrix as PIC's substrate. For this multi-implant strategy has been adopted with Carbon (C⁺) and Nickel (Ni⁺) ions implanted, separately. Their fluence along with ion energies are simulated/designed rigorously before the actual implantation experiments. Post implant measurements of Sheet resistance, mobility, drift driven electric fields, current-voltage, Arrhenius based activation energies, charge based transient analysis and detailed investigations of possible traps have been performed to study the viability of carrier removal scheme for the stable as well as reversible electrical isolation of this photonic integrated circuit's platform. Trap parameters identified as a result of a specialized charge deep level transient spectroscopy provides an insight about the energy levels and possible

evaluation of recombination/generation centers for effective photonic activity within the device regions. The optical loss study has also been performed to inspect the optical hindrance levels into the said InGaAsP PIC matrix. Results presented in this work have ramifications for device engineers with a special reference to the development of next generation Photonic ICs on monolithic substrate matrix.

List of Publications

- [1]. Hussain, Khurram and Shuja, Ahmed and Ali, Muhammad and Ibrahim, Zubair and Mehmood, Qaiser, "Ion-induced electrical isolation in GaN-based platform for applications in integrated photonics," IEEE Access, vol. 7, pp. 184303-184311, 2019.
- [2]. Hussain, Khurram and Shuja, Ahmed and Ali, Muhammad and Fahad, Shah, "Carrier removal and transport in photonic integrated circuit ready InGaAsP/InP substrate: Electrical and transients of charges evaluation," Materials Science in Semiconductor Processing, vol. 121, p. 105384, 2020.

The research work presented in this dissertation is based on the above-mentioned publications.

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LIST OF ABBREVATIONS AND SYMBOLS

IoT Internet of Things

CPU Central Processing Unit

RAM Random Access Memory

PIC Photonic Integrated Circuit

IC Integrated Circuit

CMOS Complementary Metal Oxide Semiconductor

AlN Aluminum Nitride

UV Ultra Violet

InP Indium Phosphide

GaN Gallium Nitride

GaAs Gallium Arsenide

InGaAsP Indium Gallium Arsenide Phosphide

LED Light Emitting Diode

InN Indium Nitride

keV kilo electron Volt

MeV Mega electron Volt

SRIM Stopping and Range of Ions in Matter

TRIM Transport of Ions in Matter

FET Field Effect Transistor

MOCVD Metal Organic Chemical Vapor Deposition

MBE Molecular Beam Epitaxy

SiC Silicon Carbide

DUT Device Under Test

PL Photoluminescence

SIMS Secondary ion Mass Spectroscopy

XRD X-ray Diffraction

AFM Atomic Force Microscopy

PECVD Plasma Enhanced Chemical Vapor Deposition

RTA Rapid Thermal Annealing

QDLTS Charge based Deep Level Transient Spectroscopy

TPV Transient of Photovoltage

E_A Activation Energy

E_T Trap Energy

N_T Trap Concentration

He⁺ Helium

C⁺ Carbon

Ni⁺ Nickel

R_S Sheet Resistivity

g Resistivity

μs Sheet mobility

n_s Sheet carrier concentration

E_g Band gap

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Chapter 1

Introduction

1.1 Introduction

In modern society and economy, all the areas and sectors are dependent on communication networks since they provide many services and applications of the internet. Internet connectivity provides support to critical infrastructures such as energy, gas, water, transportation and health. These infrastructures are critical and necessary for development and growth of developed and emerging Countries. Thus, Internet connectivity is a key enabling technology and making other processes and the use of resources more efficient [1]. There is steady rise in internet connectivity globally, this growing trend can be reflected from figure 1, where one can easily see a steady growth in number of Internet users worldwide.

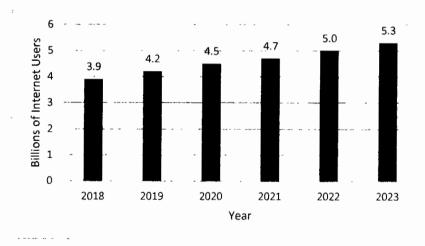


Fig. 1.1: Global Internet User Growth [2]

Majority of these Internet subscribers are coming from mobile data segment. These users are using applications such as social media, E-commerce, video games, digital advertising and Multimedia audio/video content. All of these applications are data demanding and their impact can be clearly reflected in exponential growth in Mobile data traffic as shown in Figure 2.

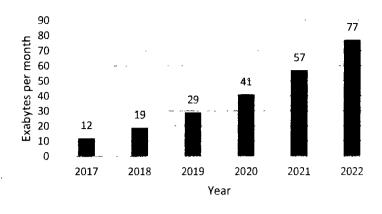


Fig.1.2: Cisco forecasts 77 Exabytes per Month of Mobile Data Traffic by 2022 [3]

In the telecommunication world, there is not only a huge increase in human connectivity, but also in human-to-machine and machine-to-machine connectivity and applications such as 5G, cloud computing services, Internet of Things (IoT), Industry 4.0, Car-to-Car communications, video connectivity etc. are getting developed and deployed with every day passing [4]. All these applications require major developments in the fields of communications which provide basic infrastructure to support these new horizons of development. One such important entity, expected to play an increasingly bigger role in the wake of such applications is Data Centers [5].

Data Centers are experiencing an exponential increase in their traffic with the rapid development of bandwidth hungry internet applications such as video streaming, big data and cloud computing. Rapidly growing demand of these applications is placing considerable load on data center interconnection networks. Presently, optical fiber point-to-point links and electronic switching fabrics are utilized to execute the switching interconnect [6]. However, in terms of performance scaling, the electronic switch chip is not keeping abreast with increase in data center traffic. For next generation, data center networks, Optical switching networks are promising candidates to provide low power and low latency communication [7].

However, the problem is not only of latency but also of power. Since increasing data rates have overwhelmed the capabilities of conventional interconnect technologies and applications such as data centers which are even more data intensive places further load on them. The main problem is that in conventional electronic data systems for communicating data between two points A and B, need to charge and discharge wires. Even in the connections between CPU and RAM chips, this charge and discharge process claims more energy and time. It is obvious that most of the energy wasted in information processing is used in communications rather than logic. Even at gate level, most of the energy is dissipated in charging and discharging of capacitance. Thus, at data-center level, the largest server farms may consume an entire power plant's worth of electricity [8].

The two major solutions which are gaining popularity among the optical communications community are Optical Interconnects and Photonic Integration. Integrated photonics is poised to revolutionize traditional electrical interconnects with the trend from long-haul communications links down to inter- and intra-chip connections [9].

1.2 Photonic Integration

Photonics involves the study of technologies used in the design of systems such as optical fibers, lasers and controlling light with precision. Light beams and lasers are main carriers in applications transmitting energy and information. Developments in the field of photonics has considerably increased the operators demand on a larger scale. This growing demand is significantly increasing the production volumes of photonic devices. Parameters such as wavelength, temperature and refractive index may play pivotal roles in the photonic devices manufacturing and fabrication [10].

An integration of multiple photonic functions which results in providing processing capability for information signals lying in the optical wavelength range is called PIC (Photonic Integrated Circuit). The hierarchy of PIC is illustrated in Figure 3.

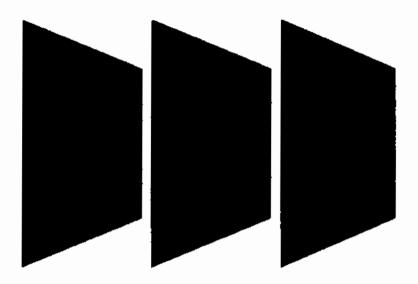


Fig. 1.3: Concept of the PICs

PICs consist of following optical components as highlighted in Figure 4.

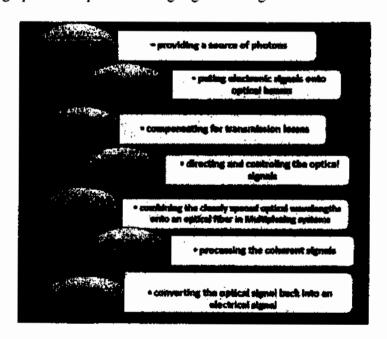


Fig. 1.4: Optical Functional Elements in Photonic Integrated Circuits

Photonic integration promises to deliver compact photonic devices with enhanced bandwidth/ switching capabilities for optical fiber communications ensuring very rapid data processing between photonic active components connected over lossless waveguides [11]. The idea of PIC was first proposed by Miller [12] in the Bell System Technical Journal:

"A proposal for a miniature form of laser beam circuitry – photolithographic techniques may permit the simultaneous construction of complex circuit patterns.... If realized economy should ultimately result".

PICs have always been economically challenged right from start, to provide same value proposition as electronic integrated circuits due to following reasons [13]:

- 1. Diversity in materials needed for photonic devices.
- Much larger size of photonic devices than electronic devices and dimensional scaling not possible
- 3. Building blocks needed for PICs are more diverse.
- 4. Circuits designs are not scalable.

In reviewing the evolution of photonic integration, many analogies can be drawn with microelectronic integration. Just as the growth in the number of transistors per chip in electronic integrated circuits follow Moore's law [14], the complexity development of Photonic Integrated Circuit (PIC) also experiences an exponential increase in past three decades. This has been highlighted in Figure 5.

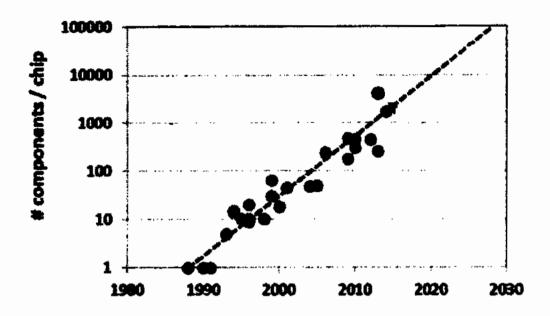


Fig. 1.5: Moore's Law in Photonics [15][15]

1.3 Photonic Integration Technologies

1.3.1 Silicon Photonics

Silicon photonics is the study of the optical properties of the group IV semiconductor and the design and fabrication of devices for generating, manipulating and detecting light. It is emerging as a powerful technology for the integration of optical functions on a chip. Silicon photonics brings optical communications into the fabrication space of the semiconductor industry, enabling low cost, high volume assembly [16]. The optoelectronic functions are fabricated on the same CMOS wafers using the same equipment and methods as electronic chips. The wafers are diced into chips just like electrical one. Optical chips can be just as inexpensive as their electrical cousins.

However, Silicon have an indirect bandgap making monolithic laser integration onto silicon PICs difficult. High performance semiconductor lasers are realized in III-V semiconductors. Therefore, there is a need for the integration of III-V semiconductors on Silicon PICs [17].

1.3.2 III-V Semiconductors for optoelectronics and photonics

III-V materials are not compatible with Silicon CMOS technology due to complexity of growth, wafer bonding issues and thermal budget. III-V Semiconductors possess unique combination of valuable properties making them highly suitable for photonic integration. Most of them have direct band gap, and hence inherently capable of emitting light. III-V Semiconductors with different band gap wavelengths ranging from the UV (e.g. AlN) to the near IR (InP). This enables light sources operating at different wavelengths. Ternary and Quaternary representatives of the class III-V offer an additional benefit of controlling the band gap wavelength, as well as adjusting the optical properties, such as refractive index and linear and nonlinear optical susceptibilities, over a wide range of values. In such a way, one can grow layers and other structural arrangement, adjusting the material compositions at different parts of the chip, such that passive and active integrated optical devices can coexist and cooperate on the same chip [18].

1.3.3 Heterogenous Integration

To address the challenge for integrated optical sources on silicon, the most promising solution so far is the introduction of III-V based lasers to silicon chips by means of heterogeneous integration. Heterogeneous approaches combine different materials on a single substrate during the process [19]. In heterogeneous integration, the pieces of III-V material are bonded onto a patterned Si Wafer and then processed together using standard lithography tools. This arrangement reduces the alignment tolerances between un-patterned III-V dies and Si Wafer. This process incorporates the superior silicon waveguide quality with smaller feature sizes achieved with the use of complementary metal-oxide-semiconductor processing infrastructure. With increase in complexity of PICs, this approach will be more important as shown in Figure 6.

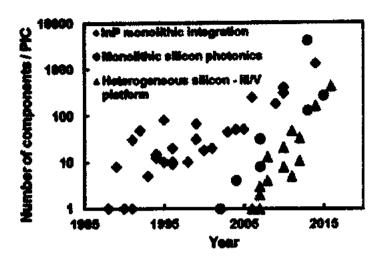


Fig. 1.6: Evolution of photonic integration in terms of number of devices in a single PIC [20]

1.4 Problem Statement

Major issue that the PICs industry is struggling with is to address the need to squeeze more transmission into a specified bandwidth, given footprint and at a given cost. As the possible solutions to meet the requirements of smaller footprint, lower power and cost-effectiveness lies in the revalidation and advancement of technology; platform or the substrate for photonic integration are becoming increasingly important. Silica-on-silicon, Silicon-on-insulators, III-V semiconductors such as InP, GaAs and their variants, and Lithium Niobate are being developed and revisited for applications in monolithic as well as hybrid integration of devices. III-V platforms have enriched the industry with their versatile applicability in photonics. Improvement in such systems by improving the performance through reduction of parasitic losses and physical delay lengths has been a focal point of current research in this area. This is predominantly being done by locally modifying the character of the III-V semiconductor (e.g. InP, GaAs, GaN or their variants) to suit the requirements of optical components. Band-gap engineering, ion-induced engineering of devices in form of electrical isolation, quantum-well

intermixing, inter-diffusion, and impurity free vacancy disordering are extensively been researched to propose such alteration for possible fabrication of efficient platforms for PICs.

Fabrication and extensive characterization of III-V platforms (InGaAsP, InP, GaAs etc.) for PICs is envisaged, in this work, where a novel combination of variety of ion-induced engineering techniques will be utilized on device matrix. This may yield an optimized process routine to make an all-implant strategy for a device scheme which would act as carrier transmitter and carrier isolator when exploited as a potential monolithic PIC platform.

1.5 Thesis outline

The overall thesis outline has crunched in the chapters as given below:

Chapter 1 describes introductory overview of the global paradigm of the Photonic ICs (PICs) industry.

Chapter 2 describes the background theory of the implantation engineering used to create the platform or matrix for PIC development.

Chapter 3 provides the recent findings published in the literature with an assessment on the key results and gaps, on the ion-engineered III-V matrix for PICs development.

Chapter 4 describes the experimental techniques used in our work in terms of design, fabrication and characterization.

Chapter 5 describes each aspect of our work comprising of experiments, results and discussion on the findings of the study.

Chapter 6 describes the summary of the findings as well as insight about the future work.

Chapter 2

Background and Theory

2.1 Introduction

In this chapter we will review the background theory of ion implantation process in the compound semiconductors. This chapter will include the fundamental concepts of the ion implantation process which will contain stopping process, issues related to implantation process in compound semiconductors, ion activation, rapid thermal annealing; various dynamics of ion implantation in group III-V nitrides and quaternary compound semiconductors and heterostructures. It will also discuss the background knowledge of n-type and p-type doping through ion implantation in GaN and another quaternary compound i.e., InGaAsP for its application in photonic integrated circuits. Similarly, the usage of ion implantation process for high resistive implant isolation in GaN and InGaAsP thin layers will be discussed. Finally, the selection of ion species for doping and isolation purpose will also be considered.

2.2 Background of ion implantation process in compound semiconductors

From the last 3 to 4 decades the group III-V based opto-electronics systems has been viewed as alternative material to replace Silicon as silicon-based circuits are reaching its miniaturization limits. The most promising compounds of III-V and its counterparts includes the N-based, As-based and AsP-based wide/direct band gap compounds which can be synthesized in wurtzite/cubic structures and zincblende polytypes. In terms of available wide band gap materials, the GaN and InN may cover most of the visible spectrum of light which makes a suitable contender for application in photonic integrated circuits (LED, Laser, detectors etc.). Due to the wide band gap the properties of the compounds, they can be tailored through doping which can be performed either by diffusion or by the ion implantation process [21]. Diffusion as a doping process is not suitable for III-V based devices because it requires extended time periods up to hours to attain the require depth in n-type doping while in p-type

GaN the diffusion coefficient is very high and strongly dependent upon the impurity concentration. Due to the above-mentioned drawbacks of diffusion, the ion implantation is the most suitable technique to tailor the properties of group III-V material-based devices. The ion implantation is the technique extensively used in the IC fabrication based on Silicon as well as the III-V based device technology. During the fabrication process a typical IC device undergoes through a series of implantation (30-40) processes with the energy ranges from keV to MeV, this technique in compound semiconductor devices is used for selective area doping/isolation purpose. In addition, ion implantation is the most suitable method to understand doping, compensation behavior, and re-deployment properties of the possible dopant species [21].

2.3 The Ion Stopping process in Compound semiconductor

The ion stopping is the process in which the implanted ions undergo through a collision process with the host atoms and loses its energy in collisions. Most of the input ion energy is transferred to the host lattices through electronic or nuclear stopping processes. The electronic stopping is related to velocity of input ion specie and to the square root of the implant energy. Nuclear stopping is related to the elastic collision between input ion and the host atoms in which the kinetic energy is transferred to give movement to nuclei. Deep level defects are generated due to the chain process inside the lattice by the successive collision that occurs during ion implantation process. In both the processes, the energy loss rate of the implanted ions is in the order of tens of eV/Å in compound semiconductors. The overall value of dE/dx is approximately constant for most of the ion's species for the specified energy for implantation. The (Straggle)Rp which is actually the projected range is proportional to the initial collision energy [21]. In the amorphous case, Gaussian stopping distribution is observed for implanted ion profile, which is proportional to the Rp, Rp and implant dose Φ are given as follows [22].

$$N(x) = \Phi * \exp\left[-(x - Rp)^2/2\Delta Rp^2\right]/\sqrt{2\pi\Delta Rp}$$
 (2.1)

The maximum concentration is represented as

$$Np = \frac{\Phi}{\sqrt{2\Delta R p^2}}$$
 (2.2)

Hopping at Rp with at a complete depth follows as

$$N(x) = N_p / \sqrt{e}$$
 (2.3)

Where the total penetration depth in Equation 2.3 is $x=R_p+\Delta R_p$

The channeling effect occurs when the ion hits a cluster of atoms and goes much deeper than the projected penetration depth, normally happen in single crystal grown targets. The right placement during the implantation process may minimize the channeling effect. The light ions are stopped at lower depths during implantation due to the electronic effects while the heavy ions are stopped at much deeper level due to the nuclear effect [21]. These heavy ions specially in III-V compound semiconductor platforms may follow a collision cascades, which leads to a huge amount of lattice damage in lower volumes. These defects are proportional to, the ion concentration, ambient temperature and the ion energy during implantation. In III-V based materials, defect/damage accumulation and respective amorphization are modeled by either a heterogeneous way (InGaAsP), in which each and every damage clusters are of amorphous nature and the complete amorphization occurs when all these regions are overlapped. In the homogeneous (GaN) case when bombarded with lighter ions, the crystal breakdown occurs and reaches to a critical level where it becomes unstable and turns to amorphous state. Note that for a specific ion to fully penetrate through a highly doped semiconductor film and render it semiinsulating, the important thing is respective ion damage profile, not itself the ion profile which penetrates. The dopant and damage profile both can be simulated by (Stopping and Range of Ions in Matter (SRIM)/ Transport of Ions in Matter (TRIM) simulation tool based on Monte

Carlo calculations for ion stopping processing as well as the distribution at required penetration depth [23].

2.4 Dopant activation by Annealing

To obtain dopant activation implanted through the ion implantation process, to minimize the compensation defects and to carry the interstitial dopant atoms into their respective lattice sites annealing process is important after the implantation process. The dopant activation rates and highest doping magnitude in III–V compound semiconductor materials are strongly dependent on the type and density of point defects which remain active after the implantation and may be the annealing process. One possible solution to solve this issue is the co-implantation in which a huge number of lattice sites are generated to be occupied during the annealing process. Similarly, the residual imperfection in the III–V semiconductor materials will indemnify the electrical dopants activation. The major issue in III-V compound semiconductors is that the lattice elements may differ from each other some may be notably lighter than the other sites i.e. Ga and N in GaN, due to which the non-stoichiometric composition takes place and the recoil mechanism is different for each incorporated lattice sites. In most of the cases, a co-implant of the host lattice site may be used to enhance the possession by the implanted ions [24].

2.5 Rapid Thermal Annealing Process

As we know that after the ion implantation process the implanted ions occupy random positions on lattice sites and there exist a lot of damages due to the ion stopping process. So, a rapid thermal annealing/post implant annealing is required to activate the dopant by short diffusion and to repair the damage produced during the implantation. The fundamental rule is that, first the damage must be recovered then the dopant activation process may occur. Up to a specified annealing temperature the films may behave highly resistive (Isolation) but when heated at

high temperature according to the two-third rule of melting point the majority of the carrier activates i.e. GaN annealed at 1100-1700°C optimum activation takes place [23]. For III–V materials high-temperature and annealing for short duration gives better electrical results, which also minimize film degradation, dopants atoms redistribution and mobility variations. But at high annealing temperature specially in GaN, GaAs, InP and InGaAsP and encapsulation layer must be deposited to minimize the surface dissociation. These encapsulation layer may be a di-electric layer or AIN which have high thermal expansion co-efficient and can be removed by etchant solution after the high temperature annealing process [24].

2.6 History of GaN Doping and Isolation Through Ion Implantation

The first research studies on ion implantation was done by Amano et al. in early 1991 in which they have studied the optical properties of implanted GaN array using photoluminescence spectroscopy [25]. They were the first research group to identify Mg as a shallow acceptor doping impurity. Pearton et al., were the first to successfully activate Si and Mg dopant in GaN substrate in 1995 both n-type and p-type [26]. After that the Oxygen and Ca showed promising results as a donor and acceptor impurity, respectively [27]. Up to now many GaN based devices has been investigated using implantation doping or for inter/intra device which includes FETs, LEDs, PIN diodes and UV detectors. It is observed that annealing dynamics and respective is poor for GaN up to 1100°C with low fluence and the extended defects remains active, while the high fluence leads to surface amorphization [28].

2.6.1 N-type doping in GaN

Normally undoped GaN grown on sapphire substrate by (Metal Organic Chemical Vapor Deposition) MOCVD or (Molecular Beam Epitaxy) MBE method is used for ion implantation with undoped carrier density in the order of 10¹⁶ cm³. The ions species are implanted at room temperature with dose of 10¹⁵ cm⁻² to obtain n-type GaN. Si is the best choice to achieve n-

type doped areas in GaN with subsequent activation with deployed annealing cycles [28]. An effective capping mechanism (AiN, SiC) is necessary to prevent GaN dissociation and high annealing temperature. The capping layer is then removed by etching solution and then the samples are characterized [29]. The results in the literature shows that Si is the more suitable dopant for obtaining n-types GaN with optimum carrier densities and mobility values. However, there are also many other group VI-based materials which may act as a donor i.e. Se, S and Te, which can also be used like Si for GaN doping.

2.6.2 P-type doping in GaN

After a detailed review it is concluded that p-type doping in GaN is a challenging task, the chance of getting any success is slim. However, the best choice in this scenario is Mg (Magnesium) which act as a p-type dopant in GaN [30]. The key issue with GaN is the absence of shallow acceptors levels. Even if we substitute Mg on Ga site in a deep acceptor level in the scenario of hole localization is stronger on it, so the available states would not behave so effective in shallow levels due to low effective mass. Somehow the possibility is that the ionization energy is sufficiently minimum to introduce few free holes if the concentration of Mg is properly selected [31]. Many other materials which includes Be and C are also tried out for implant doping, but the re-distribution of these species takes place at very slow rates and the defects remain mostly as they were present in as-implanted case [32].

2.7 Isolation in Nitrides (GaN) Via Implantation

Normally ion implantation process is done for two objectives, first for the doping and second for isolation [23]. The ion implantation for doping purpose is already been discussed in the previous section. Implant isolation is the reverse process of doping in which ion implantation is performed for the creation of highly resistive selective regions due to the formation of deep level compensation centers. In compound semiconductors, nitride-based devices this isolation

method has been extensively used for inter-device and intra-device isolation such as in photonic integrated circuits (PIC), transistor and laser etc. There are two compensation mechanism of implantation process in nitrides. It may be either by chemical or by purely damage mechanism, these mechanisms sustain the original morphology which is not possible in mesa isolation [23].

2.7.1 Damage Related Implant Isolation in GaN

In this type of ion implantation mechanism, the input ions (heavy ions) are implanted with high energy to break host material atoms from lattice sites. In GaN most of sustainable isolated regions are created using this mechanism. The damage accumulation in Compound semiconductors utilizing heterogenous models, however individual layers are simulated as homogeneous models. The complete amorphization is modeled with the overlapping of individual layers staking with respective damage concentrations. The extended dislocations or complete amorphization totally depends upon the implanted ion concentration, ion energy and the chamber temperature. Now once the isolation is created the most important thing is to check the sustainability of these isolated regions at various annealing temperature. The chosen ion species for damage related implant isolation in GaN includes H⁺ [33], He⁺ [33], O⁺ [34], N⁺ [35] and may also include inert gases. The heavy the ions the high the energy the more damage they may create [36]. There is another way through which one can achieve the most stable isolation is that if two different ion species are implanted simultaneously [37].

2.7.2 Chemically Induced implant Isolation in GaN

The rule of thumb for chemically induced isolation is that the ions species must be electronically active in the GaN band gap and normally, low dose is required for the isolation. Typically, the sheet resistances are the parameter of interest calculated using the Hall setup. The recorded values in literature for sheet resistance are normally in the order of 10¹² ohm/sq with most of implanted species. The maximum recorded value being obtained after 400-650°C

post-implant annealing. Beyond this annealing temperature the sheet resistance drops down and tends to reach its un-implanted value. The ion species that are investigated in literature are V, Ti, Fe, Cr, and O for both p- and n-type GaN layers [36].

2.8 Implant Isolation in InGaAsP

Indium gallium arsenide phosphide (InGaAsP) is a quaternary compound semiconductor material and an alloy of indium phosphide and gallium arsenide. The compound has variety of applications in photonic and opto-electronics, because the band gap can be tailored by changing the composition. Photonic integrated circuit (PICs) based on InP used different composition variation of InGaAsP to construct different photonic structures. For high performance PICs based on III-V materials ion implantation induced device isolation is a key technology for intraand as well as inter device isolation. The advantage of ion-implantation induced-isolation is the lateral-selectivity, constant surface planarity and best reproducibility. To convert highly conductive layer to highly resistive ones or to improvise the isolation, the implantation parameters such as ion specie, density, implant energy and the underneath substrate temperature are important factors [23]. A lot of research work has been done on n-type InP/InGaAs implant isolation. Stable thermally stable isolations are achieved with He+, B+, and N+ in InP n-type doped [38]. Few examples are listed for n-type InGaAsP implant isolation in literature in which material like F+, He, Si and Zn are implanted to get the high resistive layers. The right choice of implant energy, dose, ion specie and the post implant annealing are the key parameters to be chosen correctly for sustainable stable isolation [39].

Chapter 3

Literature Review

3.1 Introduction

The recent trend in the miniaturization of electro-optical and photonic devices based on III-V nitrides/Phosphides (GaN, InGaAsP) requires the precision, control and the exact position of external atoms/ions introduced to the devices through the ion implantation process. But there is various limiting factor which directly affects the process of introducing new atoms into specified lattice location inside the device under test (DUT) which may be a photonic integrated device. These limiting factors includes the spatial resolution, ion straggle, ion channeling and the broadening of the volume of implanted specie through diffusion process [21]. Similarly, all these factors may cause intentional/unintentional damages in the form of lattice deformation because the high energized ion when hit the host atoms breaking the bonds and producing various defects densities. The ion implantation in this research work is performed for main two purposes. The first purpose is to choose the specific specie of ions in order to get the desire doping density and the second cause is to create isolation region to minimize the intra devices leakage for proper operation PIC. Numerous research groups have performed different routines to investigate the effect of annealing dynamics on various implant species for doping and device isolation. In this chapter a brief literature review is presented upon the dynamics of ion implantation in order to properly understand and choose the best possible options for ion species, Ion density and suitable annealing routines.

3.2 Implant Isolation and doping in GaN

Doping of semiconductor is a versatile technique to tailor the electrical and optical properties based on its required application. GaN can be doped either n or p-type through ion implantation technique. N-type doping in GaN is easy as compared to the p-type doping through the ion

implantation process. Similarly, the underneath substrate dynamics plays a key role in terms of various parameters like thermal conductivity, bonding nature and lattice mismatch. Many research groups in the previous two decades have done some quality research on GaN growth, substrate dynamics, doping/isolation and subsequent annealing dynamics to activate dopants and to check the sustainability of isolation.

For example, M. Coig et al. have studied the n and p-type doping of epitaxially grown GaN over silicon substrate. Also, the effect of annealing temperatures in terms dopant activation vs dose of implant species and the substrate effects are investigated. For n-type doping silicon different routine of ion energies and doses are considered. The ion energies include 50, 100 and 20kev with respective ion doses from $3x10^{14}$ to $3x10^{15}$ cm⁻², respectively. For p-type doping Mg ions with dose of $1x10^{15}$ cm⁻² and implant energy of 100keV is implanted to a penetration depth of approximately 100nm calculated using SRIM. Conventional 4-point probing, Vander pauw based Hall measurements and Micro-Photoluminescence systems were deployed to study electrical/optical properties before and after ion implantation [40]. The electrical characterization results are summarized in Table 3.1 below.

Table 3.1: Electrical characteristics of GaN as a function of dose and annealing temperature [40].

Si dose (at.cm-2)	NS (cm-2)	Rsh (Ω/sq)	% activated dopant : NS/dose
3x10 ¹⁴	1.7x10 ¹³	6365	5.6
1x10 ¹⁵	4x10 ¹⁴	275	39
3x10 ¹⁵	1.9x10 ¹⁵	48	60

For p-type the characterization is done through the photoluminescence (PL) because the electrical characterization may show that the GaN films are n-type doped. It is due to the fact

that nitrogen vacancies, structural imperfections and lattice mismatch un-intentionally shows n-type behavior. The results of low temperature PL characterization are shown in the Figure 3.1 below:

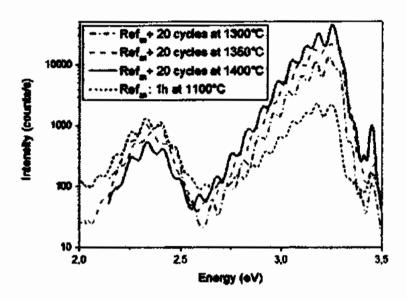


Fig. 3.1: low temperature photoluminescence characteristics of Mg doped GaN with dose of 1x10¹⁵ cm⁻² in order to investigate p-type behavior [40]

As obvious from the Figure 3.1 three PL peaks are observed, the green representing N vacancies at 2.35 eV, the 2nd peak at 3.27 in UV range is showing the Mg dopant acting as a luminscence centers while the final peak at 3.45 eV is representing the various recombination processes occurs inside the GaN itself [40].

Another research group on III-V materials funded by the national rerearch foundation korea lead by F.T. Johra have domontrated the effect of ionic species when ion implanted in GaN. The GaN thin films were fabricated using MOCVD method and the ionic species H+, He+ and Ar+ were implanted to obtain doping/isolation inside the GaN substrate for high power devices. The beam energy of 60 and 120 keV was chosen for each ion species with ion flux of 1x 10¹² and 1x10¹⁵ cm⁻²s⁻¹, respectively. After the implantation the sample were annealed from 100 to 500°C and the analysis is done for the doping type and isolation sustanibility [41]. The overall summary of implantation routine, dose and ion flux are given in Table 3.2.

Table 3.2: Conditions for ion implantation process [41]

Sample name	Implant energy (KeV)	Ion flux cm ^{-2.} S ⁻¹
A	60	1x10 ^{t2}
В	60	1x10 ¹⁵
C	120	1x10 ¹²
D	120	1x10 ¹⁵

Beased on characterization techniques results they concluded that the electrical resistivty is proportional to implanted ion flux and the input ion energy as shown in Figure 3.2 below. Room temperature resistivty calculated using the electrical analyzer tool ranges from 1×10^{-2} to $17.7\times10^{-2} \Omega$ -cm. The higher sustainbility is achieved for the samples implanted with He⁺ ion as we can see from the Figure 3.2 when annealed at 500°C still the resistivity is very high as compared to other samples. The comparision is also done for both the p-type and n-type sample with same annealing routine applied. The results for both the cases are shown in Figure 3.2 and 3.3 below:

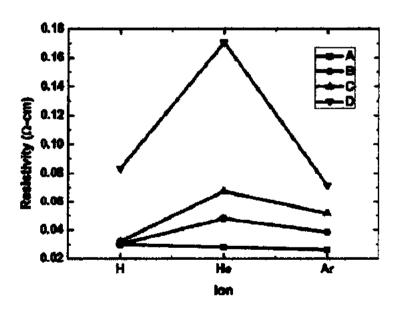


Fig. 3.2: Effect of ion flux, ion energy on overall characteristics of n-type GaN samples [41]

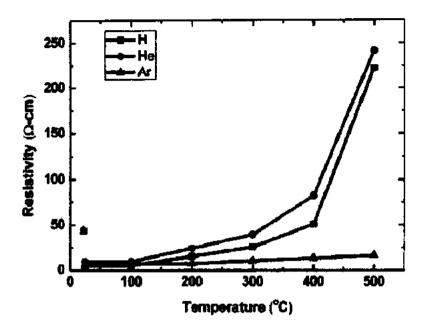


Figure 3.3: change in the resitivity of p-type samples vs the annealing temperature [41]

From the above twin plots, they concluded that for n-type samples the high resistivity was obtained through He+ implant. The H+ ion showed the anomalous behavior which can be used in practical application. While in contrary Ar⁺ also has shown better results while for p-type the resistivity shows abnormal results which will require further study to fully understand the peculiar behavior [41].

K. Kubota et al. used both similation and experimental tools to understand the displacement of lattice when Zn⁺ ion are implanted in GaN substrate. Simualtion tool TRIM/SRIM based on Monte Carlo algorithm was used to study the effect of input ion energy and flux on the penetration depth and vice versa. After physical implantation the samples were characterized by Rutherford backscattering spectrometry and photoluminescence spectroscopy [42]. Three different energies 300, 500 and 700 keV are chosen based on TRIM calculation with respective ion doses of 2.32×10^{14} , 3.02×10^{14} and 4.02×10^{14} cm⁻² respectively as shown in Figure 3.4.

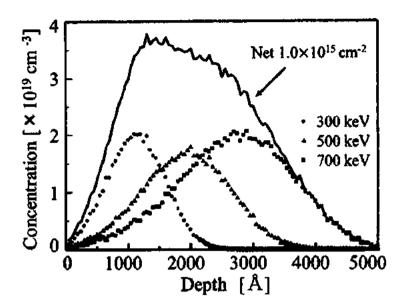


Fig 3.4: Zn ion implantation, concentration vs the penetration depth profile at multiple energies [42]

The PL analogues shows the behavior of without implant, as-implanted and annealed at 700°C samples. The yellow luminescence intensity at 530 nm is gradully increasing when increasing the annealing temperature which is the signature of gallium vacancy is acting as acceptor while the Nitrogen vacancy as a donor as shown is Figure 3.5 below for all the cases discussed.

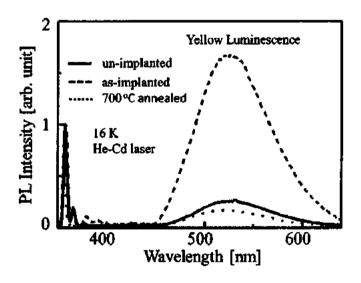


Fig. 3.5: PL spectra measured at 16k for un-implanted, implanted and annealed at 700°C [42]

The isolation like behavior is studied using the parameter called the sheet reisitance calculated using the Van Der Pauw mehtod by Hall effect system. The sheet resistance values for un-

implanted and for as implanted samples are calculted as 1.02×10^{02} , $3.98 \times 10^{09} \Omega/\text{sq}$. The sheet resistance gradully decreased to 3.7 Ω/sq when by following the whole annealing routine to 700°C [42].

T. Niwa et al. have used the conventional rapid thermal annealing method in order to obtain the highest activation ratio of Mg ion implanted in GaN. The implantation energies includes from 80 keV to 230keV with the ion doses of 9.2x10¹³ to 3.2x10¹⁵ cm⁻² repectively. The Hall effect, XRD and RBS characterization techniques were used for characterization of samples at various annealing temperatures. The penetration depth calculated by SIMS simulation was 250nm so the thickness for the Hall measurements would consider upto how much depth the Mg⁺ ions are reached during the ion implantation process. As one can see from Figure 3.6 that the hole concentration is totally dependent upon the Mg ion dose after annealing at suitable annealing temperature for specified time interval. They also concluded that the highest hole concentration of 2.1x10¹⁷ cm⁻³ was obtained for the Mg concentration of 2.1x10¹⁴ cm⁻² with the activation ratio of 2.3% [43].

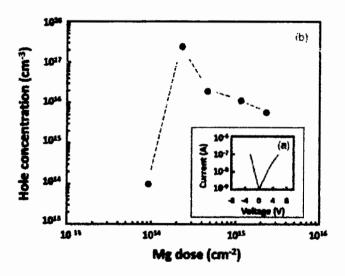


Fig 3.6: The relation between Mg dose and the concentration of holes at subsequent anealing cycle calculated using Hall method [43]

A lattice oriented distortion of 0.6% is observed which is obvious from the peak in the XRD spectra in Figure 3.7 below:

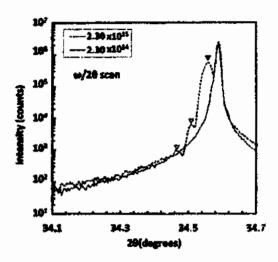


Fig 3.7: XRD spectra of GaN sample with the ion doses from 2.3x10¹⁴ to 2.3x10¹⁵ cm⁻² after annealing [43]

S. Surender et al. have done a case study research on MOCVD grown InGaN/GaN over sapphire substrate by implanting Nitrogen ion inside the heterostructure structure. Three sample were chosen for ion imlantation with the ion beam energy of 50 keV and fluence of $1x10^{15}$, $2x10^{15}$ and $3x10^{15}$ cm⁻², respectively. After the implantation for activation of implanted species the sample were annealed for 15 minutes in Nitrogen ambient at 650°C. For the understanding of ion distribution/profile after implantation and penetration depth the TRIM simulation tool was used by them. For structrual, electro-optical and morphological characterization the XRD, Hall effect, Photoluminescence and non contact mode of AFM characterization tools were used respectively [44]. The Hall measeurements based electrical characterization and AFM based parameters are listed in Table 3.3 below.

Table 3.3: The electrical and morphological properties of as grown and annealed samples [44]

S.No	Sample code	Resistivity (Ω-cm)	Mobility (cm ² V ⁻¹ S ⁻¹)	AFM roughness (nm)
1	Pristine	2.92 x10 ⁻³	415	1.3
2	1	3.589 x10 ⁻³	421	1.8
3	3	8.372 x10 ⁻²	310	3.4

4	5	4.078 x10 ⁻¹	235	5.8
5	1a	0.261 x10 ⁻³	442	1.4
6	3a	1.012 x10 ⁻³	451	2.8
7	5a	3.824 x10 ⁻³	463	3.2

For the understanding of defect and N⁺ ion distribution the Photoluminescence analysis is done for all samples at room temperature and the results are shown in Figure 3.8 below.

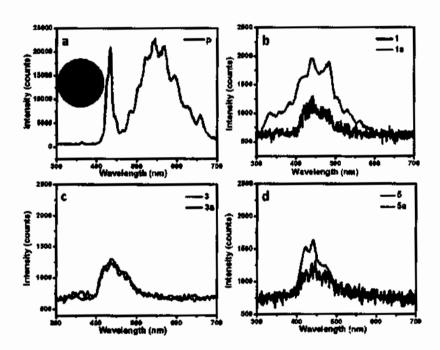


Fig. 3.8: PL analysis of (a) pristine (b) implanted with 1x10¹⁵ cm⁻² (c) 3x10¹⁵ cm⁻²(d) implanted dose of 5x10¹⁵ cm⁻² [44]

As one can see from Figure 3.8 (a) blue emission accurs at 433 nm while the broad emission from 500 to 650 nm is attributed to native defects normally cosidered to be N vacancies. After the ion implantation the passivation of active luminescence occurs which is the quenching of yellow luminescence due to damages produced during the ion implantation process. The band to band emission becomes more obvious when the samples are annealed in N ambient for 15

mins at 650°C which can be seen in Figure 3.8 (c,d) caused be the reduction of damage concentration [44].

G. Husnain and M. madhuku studied the effect of ion implantion on epilayers of GaN (2 μm) layer grown by MOCVD method over sapphire substrate. The n-type GaN was implanted with two different ion species Co⁺ and Cr⁺ at room temperature with the varities of fluences which includes 3x10¹⁶ and 5x10¹⁶ ions cm⁻², respectively. An annealing routine is carried out from temperature ranges of 700°C to 900°C for 15 min for each case only for some sample the annealing time is varied but the temperature range was kept contant. The High resolution XRD pattern shows the sattelite peak which is the signature of ion induced damages at the lattice sites. While these peaks dissappears when consective annealing cycles which is the justification lattice reconstruction and damage healing [45].

A.G. Jacobs at el. have devoloped a new caping methodology to prevent the dissociation of P-type GaN at subsequent annealing temperatures because without capping the p-type GaN shown analomous behavior [46]. The GaN samples used in their research were grown by state of the art MOCVD and PECVD mehtods. Six different varients of ion implantation routines were followed with same dose and different implant energies of Mg specie. Photoluminescence spectroscopy analysis was done for un-implanted, implanted, with capping and annealed at 1000-1300°C and the results are shown in Figure 3.9 below:

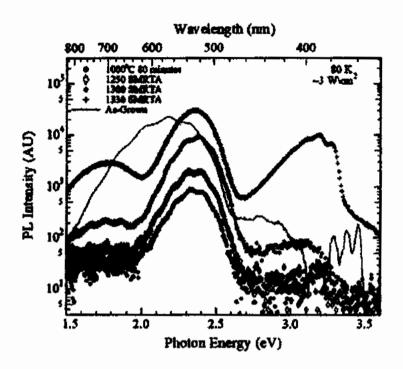


Fig 3.9: PL analysis of as grown, as implanted and annealed samples of p-type GaN [46]

The figure clearly demonstrate the activation of dopant atoms (Mg) and the compensation of defects in the as implanted samples as well as capping with different material and by following the annealing treatment. The intensity is quenched for the as grown sample with capping but by subsequent annealing an intensity shift is observed from yellow to green associated with related doping densities [46].

Y. Jiang et al. have developed a GaN based MOSFET devices with boron ion implantation based isolation as well as conventioal mesa isolation for characterization. The samples were grown by MBE method on sapphire substrate without doping and Si doped intentionally [47]. Multiple structure hierarchies, planner and circular MOSFETs were developed with specific locations isolated by ion implantation and mesa etching. The samples were annealed on 300°C for 10 mins to check the isolation capabilities for both the isolation mehtods. The conditions for developement of all specified cases are listed in the table below.

Table 3.4: Different isolation structures and implantation condition for n-GaN MOSFETs [47]

Type of isolation	Implant condition
Mesa	Un-Implanted
Ion implantation	110 keV/5×10 ¹⁴ cm ⁻² , 30 keV/7×10 ¹⁴ cm ⁻²
Both	110 keV/1.4×10 ¹⁴ cm ⁻² , 30 keV/1×10 ¹⁵ cm ⁻²
Both	110 keV/5×10 ¹⁴ cm ⁻² , 30 keV/7×10 ¹⁴ cm ⁻²
	Mesa Ion implantation Both

Upon characterization the circular MOSFET devices shows the least current density of 6.2 x 10-12 A means there exist no parasitic inside the boron implanted region. These results shows the successful fabrication of GaN based MOSFETs through boron ion implantation [47].

J. Moereke et al. have done a comparitive analysis of Fe and B implanted AlGaN/GaN hetrostuructures isolation. The AlGaN/GaN heterostructure was grown by MOCVD method on (0001) Al₂O₃ substrate [48]. The overall structure was composed of Fe implanted high resistive 4 um GaN, doped 300 nm GaN layer and 25 nm undoped AlGaN layer with sheet resistance 480 ohm/sq calculated by Hall method. For selectivity of proper implant dose and energy SRIM/TRIM simulation were carried out before implantation. The best choices were with same dose of 1x 10¹⁴ cm⁻² for both Fe, B and implant energies of 20 keV and 10 keV simultaneously. After the ion implantation process the samples were annealed at multiple temperatures for variable duration of time intervals. Low Ampere resolution current-volatage setup was used to found out the electrical properties of the isolation region as shown in Figure 3.10 below.

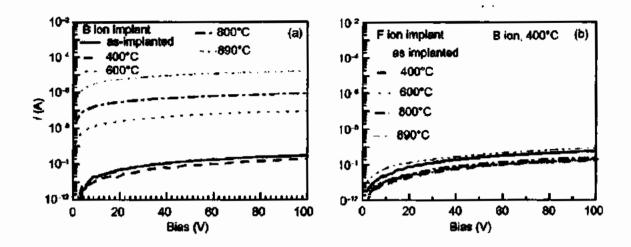


Fig 3.10: IV characteristics of both Fe and B implanted samples with annealing at different temperatures [48]

As can be seen from the Figure 3.10. That all the implanted cases discussed above the annealing current first decrease with low annealing temperatures and then it increases when the samples were annealed at higher temperatures. Similarly, for all the cases the leakage current value is the lowest at 400°C annealing temperatures [48].

M. Takahashi et al. have investigated the effect of Mg and F ions upon the electro-optical properties of GaN films grown by VP-MBE method [49]. To minimize the implant related physical damages the AlN cap layer is deposited on both sides of the GaN samples by PECVD method. Mg ions were implanted with implant energies of 40 and 100 keV with respective doses of 2.3x 10¹³ cm⁻² and 1.3x10¹⁴ cm⁻². The total ions distribution for Mg Ions calculated by SRIM/TRIM is given in Figure 3.11.

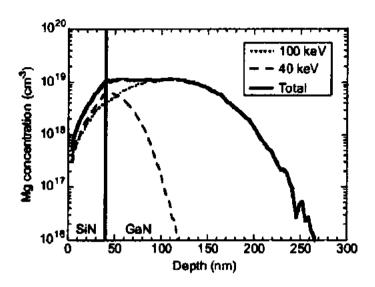


Fig 3.11: Mg ion distribution profile inside GaN template [49]

Similarly, the Fe ions were also implanted both on room temperature and high temperature with the following condition shown in Table 3.5 below.

Table 3.5: Summary of ion implantaion for Fe ions [49].

Fe ion density (cm ⁻³)	30keV/cm ²	80keV/ cm ²
1 x 10 ¹⁸	2.9x10 ¹²	1.3 x10 ^{t3}
5x 10 ¹⁸	1.4x10 ¹³	5.8 x10 ¹³
1x 10 ¹⁹	2.9 x10 ¹³	1.2 x10 ¹⁴
3x10 ¹⁹	8.6 x10 ¹³	3.5 x10 ¹⁴
5x10 ¹⁹	1.4 x10 ¹⁴	5.8 x10 ¹⁴
1x10 ²⁰	2.9 x10 ¹⁴	1.2 x10 ¹⁵

For optical characteristics the PL analysis shows yellow luminescence peak at 2.1 eV for 900°C annealed sample which is associated with the donor accepter recombination at N sites for Fe implanted samples. Also, the near band emission at 3.47 indicates high crystallography of

sample. The donor acceptor (DAP) emission at 3.28 eV is due to the activation of Mg⁺ ions implanted [49].

3.3 Implant isolation and doping in InGaAsP

Indium Gallium Arsenide Phosphide (In_{1-x}GaxAs_{1-y}P_y) is quaternary alloy in compound form and has the variety of application in electrical and optical regime. The diversity in application is due to its wide band gap which can be tailored related to the required application. Photonic integrated circuits (PIC's) based on InP, normally its alloys are used to construct lasers, waveguides, photonics cavities and quantum wells. Many photonics devices i.e., photo detectors, lasers and short distance communication systems which works in the near infrared (1500 nm) regime utilize these alloys. Now due to the trend of miniaturization of these devices on a single IC platform inter device and intra devices isolation is a critical issue during the fabrication of such devices. Similarly, the doping of such device through ion implantation is a crucial task due to residual damages produced inside the lattice sides as well as the activation of dopant atoms at the host atoms. Many researchers throughout the globe have tackled this issue by applying various techniques in which some are listed in this literature review section. A. Feckecs et al. have grown InGaAsP (1.5 μm) over InP substrate using MOCVD method for utilization as terahertz Antenna system in PIC [50]. Some specified location inside the whole wafer were implanted with Fe+ ion using Tandetron 1.7 MV accelerator. First, the simulation tool SRIM was used to understand the ion distribution and penetration depth. For practical application the ion dose of (0.1,0.2,0.3,0.4,1) ×10¹⁵ cm⁻² and the implant energies of (0.25,0.5,1,1.8,2.5) MeV were chosen based on the simulation results. All the wafers were then checked for electrical/optical and damage analysis before and after ion implantation. The annealing routine was set from 400°C to 800°C for all samples for 15 minutes. The electrical/optical characterization results found out using the Hall effect/PL systems are shown

in Figure 3.12. The most suitable results for their respective application (dipole antenna) has been achieved at annealing temperature from 500°C to 600°C. These results include the electrical resistivity of 1200 to 2500 ohm-cm, electrical mobility of 400 cm² V⁻¹s⁻¹ and the emission spectra of 1515 to 1775 nm calculated using PL system.

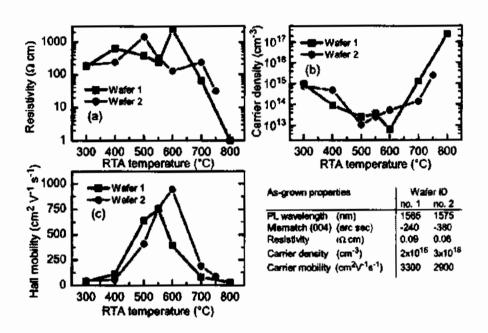


Fig 3.12: effect of RTA annealing (400-800C, 15 sec) upon the electrical characteristics of Fe implanted sample (2.1x10¹⁵ cm⁻²) [50]

The Figure 3.12 indicated that initially huge amount of damage was produced during the implantation process as indicated through the mobility plot. The mobility was too low at lower temperature ranges but become more obvious when the annealing temperature were increased, and the channel are built up for charge carrier's transportation [50].

M. Xaio et al. have investigated the effect of RTA on the performance (Optical) characteristics of lnGaAsP based quadruple-junction solar cells developed by the Molecular Beam Epitaxy (MBE) technique [51]. The lnGaAsP films with the thickness of 1μm was grown on lnP substrate with doping density of Be 2x10¹⁷ cm² through MBE. Samples were then annealed at two different temperature (700°C, 800°C) for few seconds. For photoelectrical characterization

the continuous wave PL (CWPL) and time resolve PL (TRPL) was used. The obtained results from both the techniques are shown in Figure 3.13 below:

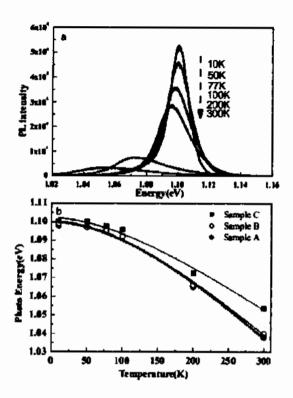


Fig 3.13: Annealing temperature dependency of (CWPL) PL spectra of InGaAsP/InP for all cases discussed in terms of doping and luminescence type [51]

The Figure 3.13 shows the red shift with increase of temperature and the respective FWHM go on increasing. While on another side the Stokes shift occurs at 77K which is related to material quality as the sample C shows lower Stokes shift. The TRPL results are shown in Figure 3.11 for the calculation of PL decay. The decay time is how fast/slow a luminescence center generated intentionally or un-intentionally emits light in the form of photon to the outer environment. The decay time for all the cases sample C at 800°C shows a longer decay time while the other samples show faster decay.

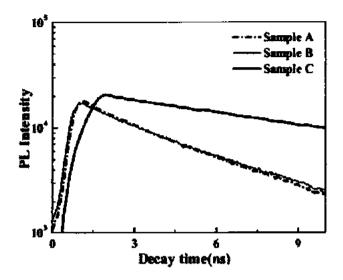


Fig. 3.14: TRPL analysis of samples when excited with 5mW excitation source at 10K [51]

Based on the results shown in Figure 3.14 that there exist a lot of non-recombination center inside the InGaAsP in as grown form. These recombination centers are decreased when the annealing temperature is increased to 800° C which alternatively increases the quantum efficiency of the device matrix [51].

B. Ilahi et al. have developed a semi-insulation platform for photonics application (1300 nm) based on InGaAsP/InP using OMBE method [52]. The device has the band gap of 0.95 eV with 1000 nm thickness and is doped n-type un-intentionally. For tailoring the properties by ion implantation process Fe+ was chosen as deep level impurity specie to be implanted using TRIM/SRIM simulation tool. Fe+ was implanted with different implant energies ranging for 250 to 1800 keV with respective ion fluence of 0.12 to 1.12×10^{12} cm⁻² respectively. The Hall measurement are carried out for all the cases before and after implantation and the results are shown in the Figure 3.16 below. The Hall effect measurements showed the electrical resistivity of 0.53 ohm-cm, the carrier density of 3×10^{15} cm⁻³ and the Hall of mobility of 4500 cm²v⁻¹s⁻¹ respectively for un implanted sample. After implantation as we can see downward trend in the carrier mobility due to the damage of host lattices and its directly proportional to the fluence of Fe+ ions as well as energy.

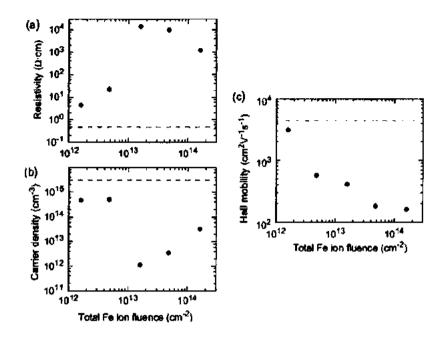


Fig: 3.16: Variation of Hall parameters before, after implantation at different dose and implant energy and after following subsequent annealing cycle [52]

The highest dark resistivity was achieved at a high ion fluence of 1.6x10¹² cm⁻² and showed temperature dependency up to 400°C with the activation energy of 0.48 eV calculated by Arrhenius analysis [52].

A Fekecs et al. have developed a critical annealing temperature based resistive heterostructures surfaces of lnGaAsP/InP implanted with Fe and Ga [53]. Two different heterostructures (band gap=1.3, 1.5 eV) were developed by implanting a high dose of ion species at MeV energies. The InGaAsP was grown on InP (0.1 um) substrate by organometallic VPE method with thickness of 1500 nm.

The implantation sequence for both the implant species are listed in Table 4.4 below. This sequence was tested using the simulation tools SRIM/TRIM before the physical implantation procedure [53].

Table 3.6: Ion implantation sequence based on SRIM calculation [53]

<u> </u>		Implantation sequence	
Implant parameters	Implantation sequence (Fe)	(Ga)	
Implant energy (MeV)	(0.25, 0.50, 1.0, 1.8, 2.5)	(0.33, 0.63, 1.15, 2.03, 3.3)	
Ion Flux (cm ⁻²)	(0.11, 0.22, 0.33, 0.44, 1)	(0.07, 0.12, 0.24, 0.29, 0.74)	
Total Fluence (cm ⁻²)	2.1 x 10 ¹⁵	1.46 x 10 ¹⁸	
Average density (cm ⁻³)	1.1 x 10 ¹⁹	7.1 x 10 ¹⁸	
Atoms displacement	6.5	5.8	

For electrical characterization the Van der pauw method-based Hall effects system was used at 300K and the results they obtained are given in Figure 3.17 below.

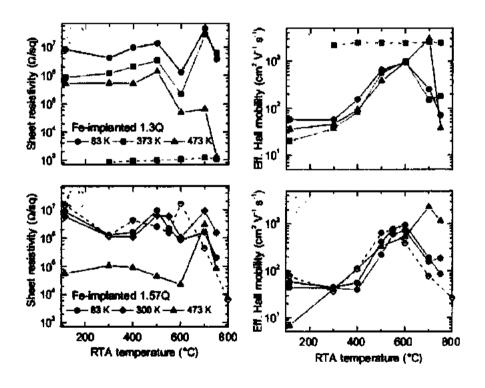


Figure 3.17: Electrical characterization of ion implanted InGaAsP films [53]

As can be seen from Figure 3.17 the highest sheet resistance in order of 10⁰⁷ ohm/sq with Fe ion implantation when annealed at 500°C and a progressive recovery of Hall mobilities are

observed above 300°C to 600°C. The highest mobility of 10³ cm²v⁻¹s⁻¹ is achieved at 600°C and a gradual decrease is observed above 600°C [53].

Y. J. Ma et al. have studied the compensation doping and its effects on recombination dynamics of InGaAsP grown by MBE method on InP substrate [54]. The sample was grown by at the InP substrate temperature 520°C with the chamber pressure of 10⁻⁰⁵ Tor. Various characterization tools i.e. Hall effect, PL and SIMS were used to characterize electrical, optical and structural properties. The results obtained from these techniques and the implantation process information are listed in Table 3.7 below:

Table 3.7: Physical parameters for growth as well as its transport properties [54].

Sample	Growth Temperature (°C)	NBe (cm ⁻³)	SIMS No (cm ⁻³)	Na (cm ⁻³)	Mobility (cm²/Vs)
B735	735	1.3E17	7.9E16	-2.9E16	203.1
B760	760	3.9E17	1.2E17	-1.7E17	111.3
B780	780	9.5E17	1.0E17	-4.4E17	71.8
B800	800	1.9E18	I.0E17	+3.3E17	28.3
B830	830	1.2E18	3.0xE16	+2.3E18	31.4

In the Table 3.7 N_{Be} are actual the counts of compensated Be atoms calculated using secondary ion mass spectroscopy. For Be atoms concentration ranging from 1.3E17 to 9.5E17 cm⁻³ that Hall measurements shows n-type behavior with doping density of 2.9E16 to 4.4E17 cm⁻³ respectively. The n-type behavior of the samples shifts to p-type when the Be concentration exceeds the previous limits [54].

V. Sadasivan et al. have developed an integrated platform based on InGaAsP/InP quantum wells intermixing [55]. For band gap engineering the ZrO₂ buffer layer is grown on the surface, looking at the solubility of In and Ga in it. The ZrO₂ is annealed to obtain two wave guided photodetector using the quantum well structure. Two optical characterization techniques PL and wave guide alignment setup were used to investigate the optical properties. According to PL analysis the Fe ion implantation is done which shows a differential blue shift in the range of different variants of ZrO₂ from 400 to 700nm as shown in Figure 3.18.

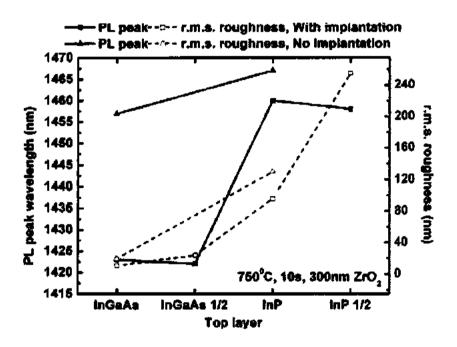


Fig 3.18: PL analysis for different ZrO2 thickness and rms value for surface roughness [55]

The graph shows a blue shift for the areas enriched with lnGaAs. The Fe implanted also shown the same trend in lower band shifting in the same condition of ZrO₂ capping and annealing temperature. A very thin layer of lnGaAs up to 10 nm is sufficient to produce variation in band gap for un-implanted condition while with Fe implantation this range extends to 30 nm with respective annealing conditions [55].

J. K. Park et al. have successfully demonstrated a variable light attenuator with PIN structure by the diffusion of InGaAsP, Ni and Zn alloys [56]. The n+ side is fabricated by the direct diffusion of Ni with InGaAsP at the annealing temperature of 350°C. While the P side is developed by diffusing the Zn at 500°C annealing after the spin coating on glass. The device is successfully tested by injecting carriers to InGaAsP layer through the PIN lateral structure. They have achieved the light attenuation of -40 dB/mm with an injection current density of 40 mA/mm at a 1550 nm wavelength [56].

A. Fekecs et al. developed a novel technique to tailor the band gap InGaAsP/InP heterostructure by MeV ion implantation of Fe for terahertz photonics devices [57]. The InGaAsP (1.5 μm) over InP (0.1 μm) was grown by MBE technique while the Fe ions were ion implanted with five different energies up to 2.5 MeV. The implantation routine was set in such a way to produce uniform damage as well as to evenly incorporate the Fe ions inside the InGaAsP at a temperature of 83K. a total fluence of 1.9 x 10¹⁵ cm² was implanted based on simulation results with 6.5 atomic depth and 0.03% Fe incorporation. The samples were then carried out through an annealing temperature of 400°C to 750°C. For characterization after annealing cycle the XRD and TEM tools were used in order to investigate the effect of ion implantation on recrystallization process. There results show that the transition of InGaAsP layer occurs into the amorphous state after multiple implantations has been done on 83K. After the annealing multiple process of recrystallization took place via SPE (Solid Phase Epitaxy) or SPR (Solid Phase recrystallization) obvious from both the XRD and TEM results [57].

J. S. parker et al. have demonstrated a material regrowth platform for PIC'S (Photonic integrated Circuit) on InGaAsP/InP with low optical losses and high gain [58]. They have developed a 2.5 x 4000 μm optical amplifier laser setup having 40 dB/mm gain at a wavelength of 1570nm with (PVL) passive waveguide losses of less than 2.3 dB/mm. A shift (blue shift) in the range of >135 nm is obtained by implanting phosphorous ions at 190 keV and at subsequent annealing of 670 °C for 2 minutes. SIMS and PL techniques were deployed to investigate the effect of dopants on ion channeling. The results show that The PL wavelengths

in the active and passive sections are 1.53 and 1.41 μ m, respectively. Lasing wavelengths for 500 μ m (FP) Fabry-Perot lasers are 1.567 and 1.453 μ m, respectively. This is the most sophisticated process for the creation of large-volume regrowth-free PICs, and for optimization of novel photonic components for fast processing time is required. By avoiding regrowth defects and interface contamination, high-yield and high-performance photonic components can be fabricated [58].

Chapter 4

Design, Fabrication and Characterization Techniques

4.1 Introduction

Normally, the diffusion process is used for the doping of most of the semiconductor devices especially for silicon-based technology. But this technique is not more suitable for group III-V based devices because, a highest diffusion co-efficient is required for p-type dopant which is also concentration dependent. The other issue is achieving the incorporated depth is n-type doping which requires extended hours and very high temperatures. Now to selectively change the properties of a specifies region inside the device, ion implantation is the most robust and suitable process. In our research work the ion implantation has two objectives: first, for doping and second for the isolation of specified region in GaN and InGaAsP based devices for photonic integrated circuits (PIC) application. The active region of the device is fabricated with Metal Organic Molecular Beam Epitaxy (MOMBE) method. This chapter is divided into several sections: detailing the design, processing and characterization techniques used in this work. Ion implantation process is simulated using the modeling and simulation software's which include SUSPRE and TRIM/SRIM. Another part of this chapter includes the theoretical and mathematical formulation of all the techniques used in this study. This also includes the brief description of research tools used in this work available in the Centre for Advanced Electronics and Photovoltaic Engineering (CAEPE).

4.2 Surrey University Sputter Profile from Energy deposition (SUSPRE)

SUSPRE first developed by Roger Webb at Surrey is a numerical solution-based simulation tool uses the Boltzmann Transport Equation to develop an approximate solution based on the range algorithm of implant species. This tool is designed to numerically calculate the implanted

specie range inside the target material and the total count of damages created during the process. Boltzmann transport equation is an analytical method to evaluate the energy transfer and penetration depth inside the solid substrate for different cross-sectional areas [59].

4.3 Stopping and Range of Ions in Matter (SRIM)

SRIM stands for "Stopping and range of lons in Matter" and TRM stands for "Transport of lons in Matter" [60]. SRIM is computer-based simulation tool used to calculate interaction of ions with matter. It was first introduced in 1980 and every six years its new version release with major updates. It is worldwide renounce software for simulating ions implantation tool shown in Figure 4.1 below:

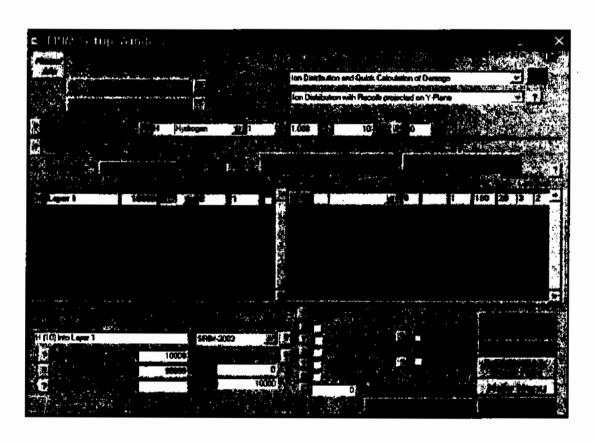


Fig. 4.1: SRIM/TRIM Setup Window [60]

Using this tool, we can select implanted ions energy, duration, and ions material types. Also, we can select numerous targeting materials. Different graphs of output can be observed at a

time related to recipe chosen. Important data are ions ranges and their straggling, different mechanisms for energy loss and their contribution, sputtering yields, damage profile and ejection energy [60].

TRIM setup window, as shown in Figure 4.1, is used to input data on the ion, target and type of TRIM calculation we wanted. It can be divided into three divisions. Ion data, target data and calculation parameters.

Ion Data: In this part, we can select type of TRIM calculations, ions types, ions energy and angle of incident. Following are types of TRIM calculation.

- Ion distribution and quick calculation of damage
- Detailed calculation with full damage cascades
- Monolayer collision steps
- Calculation of surface sputtering
- Neutron/Electron/Photon cascades
- Various ion energy/angle/positions
- Special multi-layer biological targets

In ion data, we select dopants ion types, implantation energy and ions angle of incident.

Target Data: In this region, we can select target material which can be an element or compound, target materials layers, target material destiny and we can put any name of our choice to element/compound layer. We also need to select whether it solid or gas because TRIM treats both differently.

Calculation Parameters: In this section, we can select number of ions bombarded, automatic saving of calculations and viewing window for data and plotting. Although TRIM calculates all portion of detailed analysis. In this portion, we can view a single portion of the detailed

analysis. These single parts can be Ion range, backscattered ions, transmitted ions/recoils, sputtered atoms and collision details.

4.4 Ion Implantation

lon implantation is a low temperature process in which the ions of one species are accelerated by an ion accelerator towards a target substrate in order to brought changes in its chemical, physical and electrical properties. When these ions are impinged towards the substrate, either it may reflect back or go to a penetration depth as we acquire There are three fundamental units of an ion implanter which includes the ion source, the particle accelerator and the target unit as shown in Figure 4.2. In the first unit the ion of various implant species is produced as well as in the second unit the produced ions are accelerated electrostatically while in the third unit these ions are impinged on a target substrate inside the target chamber.

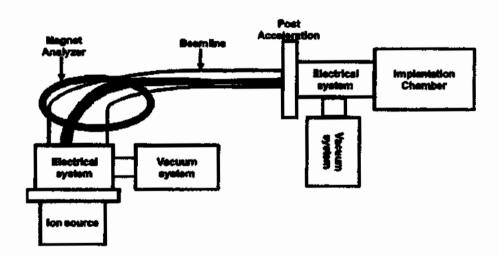


Fig. 4.2: schematic diagram of the ion implantation process [61]

In this research work the sample are ion implanted using the 5 MV Pelletron Accelerator Facility at the National center for physics [62] as shown in Figure 4.3.

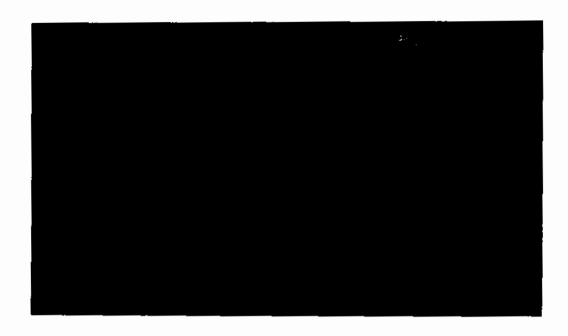


Fig. 4.3: 5-MV Pelletron Accelerator Facility at the National center for physics [56]

The system contains two types of ion sources ALPHA-TROSS and the SNICS depending upon the user requirements. The ALPHA-TROSS is basically the radio frequency (RF) ion source to implant alpha particle and proton while the SNICS uses the Negative Ions by Cesium Sputtering which can implant almost all element from the periodic table. The technical specifications are given in Table 4.1.

Table 4.1: Technical specification of ion implanter at National Centre for Physics (NCP), Islamabad, Pakistan [62]

	Specifications		
Model Number	5UDH-2		
Made in	National Electrostatics Corporation, (NEC) USA		
Max Voltage	5MV		
Charging Type	Pelletron charging system		
No of sources (ions)	SNICS, RF		
Materials	H, He, C, Si, Ni, Cu & Au		
	B. P. S will be available soon		
Beam angles	15°. 30°		
Max Beam Energy	30MeV		
Current	200nA		
Targets	6 at a time		

4.5 Electrical Characterization

As we know that electrical resistivity or in inverse the electrical conductivity is the fundamental property to understand the nature and type of any new material. Based on electrical conductivity, we have categorized the materials as a metal, semiconductor and an insulator. Semiconductor materials offers a variety of conductivities due to the dynamic's effects of free carriers' concentration in terms of doping profile. The conductivity is normally related to bulky material like semiconductors stacks epitaxial layers etc. The conductivity of a semiconductor material denoted by σ (S/cm) is proportional to its specific resistance denoted by ρ (Ω -cm) as follows [63]:

$$\sigma = 1/\boldsymbol{\rho} \tag{4.1}$$

In case where the conductivity is dominant due to the free carrier concentration then it can be formulated as follows.

$$\sigma = q\mu n \tag{4.2}$$

while q $(1.602 \times 10^{-19} \text{C})$ in Equation 4.2 is elementary charge on electron, μ (cm²/Vs) is free carriers' mobility and n(cm⁻³) represents the volume carriers' density. Now if we consider both the majority and minority carrier the conductivity equation can be re-written as follows.

$$\sigma = q\mu_n n + q\mu_p p \tag{4.3}$$

a correction factor will be included in case of thin films characterization to minimize error margin and the equation becomes in terms of specific sheet resistivity as.

$$\rho = V/I d \pi/\ln 2 \tag{4.4}$$

Where d is the layer thickness and ρ is the specific resistance [63]. There are basically two techniques to calculate the conductivity in such case which is discussed in the next section.

4.5.1 Two-point probing

As obvious from its name that only two probes are used in this case and is the simplest method. But it is very difficult in this method to calculate both the current flow and voltage drop at the same time. The system requires a sophisticated measuring system to tackle both the current and voltage at the same time. The technique is more suitable for the material/substrate with large size and high resistivity values [64]. Two probe arrangements are shown in Figure 4.4.

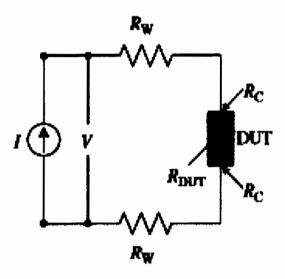


Fig. 4.4: Two measurement resistance measurement arrangement [64]

In Figure 4.4, R_W is the probe or wire resistance, R_C is contact resistance, DUT is device under test and R_{DUT} is resistance of device under test. Each contact behaves as voltage and as current probe. Total resistance R_T will be:

$$R_T = V/I = 2R_W + 2R_C + R_{DUT}$$
 (4.5)

4.5.2 Four-point probing

This technique is more suitable with low resistivity and smaller shape samples. in this case the voltage drop is measured between the two probes when these probes are not in point contact means that the distance is replaced by the sample thickness. Now when we further investigate

the materials, we concluded that the conductivity is not the only fundamental property of a semiconductor to fully understand about its behavior. Four-point probe is shown in Figure 4.5.

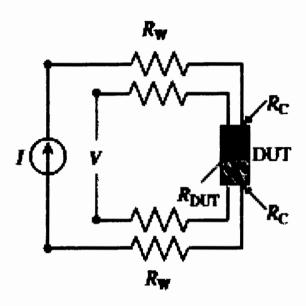


Fig. 4.5: Four measurement resistance measurement arrangement [65]

As seen in Figure 4.5, there are two additional contacts for measuring voltage. Now new voltage path also contains R_C and R_W . Due to high input impedance of the voltmeter (around 10^{12} ohms or greater), the current flowing in this voltage path will be very low. Therefore, voltage drop around R_C and R_W is too small which can be neglected, and measured voltage will be almost the voltage across DUT. So, by using four probes, we eliminated the parasitic voltage drops. This four probes measurement also frequently referred to as Kelvin measurements. The four-point probe was originally proposed by Wenner in 1916 to measure the earth's resistivity [66]. In Geophysics, this probing measurement is also known as Wenner method.

There are many other properties of material specially for semiconductors to fully understand it behavior under different circumstances like temperatures and also for different application. These properties include sheet resistance, sheet carrier density and carrier mobility etc. The information about all these properties and the characterization techniques are listed in Table 4.2.

The most important ones from these techniques are the Hall effect measurements, ultra-low resolution I-V characterization and the charge-based deep level transient spectroscopy technique.

All the mentioned techniques are discussed as follows.

Table 4.2: Important electrical properties and techniques to calculate these properties [66]

S#	Material Property	Symbol	Characterization technique
1	Specific Resistance	ρ	The Van der pauw 4-point probing
2	Electrical conductivity type	n/p type	Hall effect
3	Carrier density	n,p	Hall effect, CV analysis
4	Carrier compensation ratio	N _D /N _A	Temperature based Hall effect
5	Doping profile(depth)	N(x)	CV analysis
6	Drift velocity	V _n ,V _p	IV analysis
7	Impact ionization	σn	IV analysis (temperature based)
8	Minority carrier lifetime	T_n, T_p	IV and photoconductivity analysis
9	Trap levels related parameters	N_t , σ_n , σ_p	Q-DLTS

Before starting with Hall effect theoretical background first one must know about the prerequisites of Hall measurements which is called the van der-pauw method. This method is totally dependent upon the given sample geometry like size, shape, thickness and many more.

4.5.3 The Van der pauw method

Van der Pauw technique is used to measures Hall coefficient and resistivity of semiconductors at different temperatures. Its main advantage is that it gives accurate measures properties of sample of any arbitrary shape and is also a four-point probe method. Following measurements can be determined by this method. The geometrical topologies are mentioned in Figure 4.6 below:

- · Resistivity of material
- Sheet carrier density of majority carriers
- Mobility of majority carrier
- Doping type (n-type or p-type)

To use this technique, following four conditions must need to be satisfied [67].

- Sample must have flat shape of uniform thickness
- Sample must be isotropic and homogeneous
- Sample must have not any isolated holes

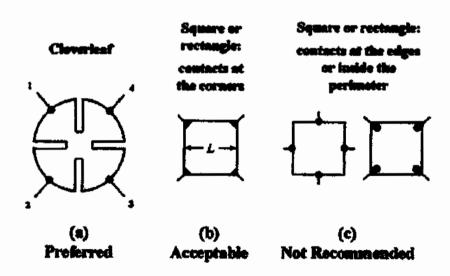


Fig. 4.6: Possible contact placements [60]

Sheet Resistance: Sheet resistance can be calculated as [68]:

$$R_s = \frac{\pi d}{\ln 2} \tag{4.6}$$

Where $\pi/\ln 2$ is Van der Pauw constant and its value is approx. 4.53236 and d is distance between two points of probes.

Hall Measurement: Hall measurement can be calculated as:

$$V_H = \frac{IB}{qn_s} \tag{4.7}$$

Where n_s is sheet density, B is magnetic field strength and I is applied current.

Mobility: Mobility is calculated as [68]:

$$\mu_m = \frac{1}{qn_sR_s} \tag{4.8}$$

4.5.4 The Hall Effect Theory

In 1879, Edwin Hall discovered Hall Effect when he was investigating the nature of force acting on a conductor which carrying a current in a magnetic field [69]. To find the electrical characteristics of any semiconductor or magnetic devices, magnetic field play an important role. Transport of properties and their properties in semiconductor can be finding through resistance and voltage. The Hall Effect measurements are basically based on Lorentz force and can be defined as "When movement of electron is perpendicular to magnetic field, a force is produced which push electrons in upward direction".

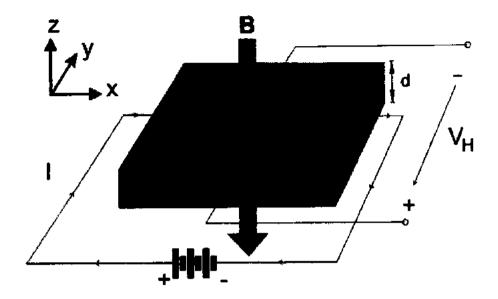


Fig. 4.7: Hall Effect in a current conducting material [70]

This force is called Lorentz Force and express as

$$F_L = q \left[E + (V \times B) \right] \tag{4.9}$$

When electrons are moving in magnetic field, they strive F_L in upward direction by making positive charges on one side and negative charges on other side, hence, induces a potential difference which is called Hall voltage (V_H) and mathematically written as

$$V_H = \frac{IB}{qnd} \tag{4.10}$$

Where B is magnetic field, d is thickness, I is current, and q is charge.

Sheet density: Sheet density (ns or Nd) can be determined as

$$ns = \frac{iB}{qV_H} \tag{4.11}$$

Mobility of the carrier:

$$\mu_m = \frac{1}{q n_s R_S} = \frac{|V_H|}{R_S IB} \tag{4.12}$$

Resistivity of the material: This is measured by applying different magnetic field strengths, the path followed by the electrons is reduced its potential over there, by the difference of voltage potential, we find out the resistivity of the material [70].

Sample Type: If the bending of carrier is towards the N- pole than p- type material and vice versa. V_H is negative for n type, while for the p-type VH will be positive.

$$V_H = \mathbf{\in} \mathbf{w} \tag{4.13}$$

$$\epsilon = \frac{IB}{qnA} \tag{4.14}$$

Where \in is Electric Field Strength and B is the magnetic field applied.

4.5.5 Current-Voltage (I-V) Analysis

A current voltage (I-V) characteristic is a technique which is used to find the current and voltage parameters of a device. As the name shows I-V curves tells the relationship of flowing current in a device to the device applied voltage. Mostly semiconductor devices except resistors have non-linear I-V curve. Current voltage curves can be grouped into different groups like active Vs passive, linear Vs non-linear, negative Vs positive resistance. It can also be used in four-point probing system to determine the sheet resistance and resistivity of semiconductor [71].

4.6 Charge based Deep Level Transient Spectroscopy (Q-DLTS)

Q-DLTS stands for "Charge based Deep Level Transient Spectroscopy". This is a charge relaxation technique which is based on the measurements of transients of trapped charges upon specific electric field. It is also use for discovering small concentration of defects and also to measure their properties. Almost every DLTS techniques are based on calculation of a transient signal (current, voltage, charge or capacitance) over range of temperatures to extract properties

of charge traps (E_t , σ_t and N_t). In case of Q-DLTS technique, it's based on measurement of transients current. His technique is quite successful for organic materials.

For measurements on Q-DLTS technique, first we determined short circuit current, open circuit current, power conversion efficiency and fill factor. Then, these values are compared to the literature values. Then, reverse biased voltage ($V_D = -0.7 \text{ V}$) is applied to device. On delay of every 10 ms, a 1 ms voltage pulse is applied to measure the current density throughout the device ($J_{D(t)}$). In case of forward biased voltage, in Space Charge Region (SCR) of device all traps will be populated. By again applying reverse biased voltage, all populated traps which are in SCR will emit captured charge carriers. After removing the influence of the reverse leakage current (J_{leak}) and capacitive displacement current (J_{cap}), the trap emission current ($J_{E(t)}$) will be obtained [72].

By the Shockley Read Hall (SRH) Model, the current produced from these emitting traps will be:

$$J_E(t) = \sum_i \frac{WN_{T,i}}{\tau_{E,i}} \exp(-\frac{t}{\tau_{E,i}})$$
 (4.15)

Where W is width of SCR, $\tau_{E,\,i}$ is emission time constant for trap type i and $N_{T,i}$ is volume density. Now, if we consider that emission of charge carrier is thermally activated process, then, the emission time constant for each trap type i can be determine as:

$$\tau_{E,i} = \sigma_{T,i}^{-1} \Gamma_{p(n)}^{-1} T^{-2} \exp\left(-\frac{\Delta E_{T,i}}{kT}\right)$$
 (4.16)

Where K is the Boltzmann constant, $\sigma_{T,i}$ is cross section of trap, T is temperature of system and $\Delta E_{T,i}$ is activation energy o trap. Γp (n) is material dependent factor which is given by:

$$\Gamma_{p(n)} = 2 \times 3^{\frac{1}{2}} \left(\frac{2\pi}{h^2}\right)^{\frac{3}{2}} k^2 m_{p(n)}^*$$
(4.17)

Where $m_{p(n)}^*$ is efficient mass of free holes and electrons and h is Planck constant. Now, total density of emitted carriers (N_E) will be:

$$N_E = \frac{1}{W_a} \int J_E(t) dt = \sum_i N_{T,i}$$
 (4.18)

Where q is electron charge. Now by calculating DLTS spectrum (ΔQ), same current transient data can be used to extract cross section (σT) and trap energy ((ΔE_T). ΔQ can be calculated by:

$$\Delta Q = Q(t_2) - Q(t_1) = \int_{t_1}^{t_2} J_E(t) dt$$
 (4.19)

Where t_1 and t_2 are two different times which can be freely chosen to define detector time constant τ_Q . τ_Q will be:

$$\tau_{Q} = \frac{t_2 - t_1}{\log^{t_2}/t_1} \tag{4.20}$$

Similarly, under the isothermal condition at room temperature the total defects concentration can be calculated from $\Delta Q(\tau_0)$ as

$$N_t = 4 \Delta O_{max}/qA \tag{21}$$

After applying the Arrhenius approximation, the activation energy E_a and capture cross-section σ of each trap can be calculated at various temperatures [73].

4.7 Transient of photocurrent/voltage

Photocurrent and photovoltage transients' characterizations of photovoltaic devices is easy to perform and its gives some very useful and important information such as charge carrier lifetime. In these techniques, the device is exposed by modulated light and photocurrent/photovoltage is recorded in frequency or time domain.

4.7.1 Photovoltage Characteristics

Transient of photovoltage is time resolve technique. This technique is based upon the excitation of device by small pulse of light. This process is performed under open circuit voltage condition V_{OC} . In this technique, device is kept in open circuit condition, constantly light fall on device and device is connected with oscilloscope. As device is in open circuit condition, So, no current can flow through device and contacts. Oscilloscope will register the change in voltage. After reaching the stabilizing of V_{OC} , device is excited with additional short time laser pulse which will cause a small disturbance of V_{OC} . The variation in V_{OC} is directly proportional to the photo generated carriers by laser pulse. As device is open circuit, this extra generated pulse will recombine which result in registration of initial transient V_{OC} as shown in Figure 4.8 [74].

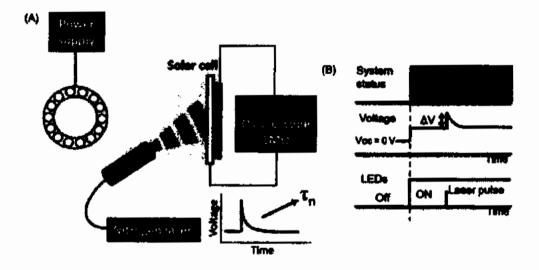


Fig. 4.8: (A) Schematic Photovoltage setup (B) Oscilloscope measurement [74]

Through the change in V_{OC} , we can extract measurement of carrier lifetime by following equation:

$$\tau = \tau_0 e^{-\beta V_{OC}} \tag{4.22}$$

Whereas τ is carrier lifetime and β is decay constant.

4.7.2 Photocurrent Characteristics

Transient of photocurrent is current response of device under short circuit conditions and its measure conditions are same as transient of photovoltage. It setup is very similar to TPV setup except that device is under short circuit condition and a small resistor is connected to it as shown in Figure 4.8 [73].

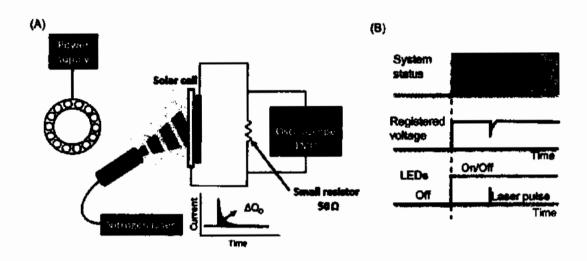


Figure 4.9: (A) Schematic Photovoltage setup (B) Oscilloscope measurement [73]

Laser pulse create disturbance in device current which will measured in oscilloscope. Voltage drops across resistor which can be easily converted into transient current by ohm's law.

4.8 Optical Characterization

4.8.1 Spectroscopic Ellipsometry (SE)

Ellipsometry come from the word "elliptically polarized light". Spectroscopic ellipsometry is optical technique which is used for metrology and analysis the dielectric properties of material. A common ellipsometry measurement has one wavelength and spectroscopic ellipsometry by using more than one wavelength has extended range of ellipsometry [74]. If two in phase light beams are combining then, it will be linearly polarized and if two out of phase light beams are

combing then, it will be elliptically polarized light. Schematic spectroscopy ellipsometry measurement setup is shown in Figure 4.9.

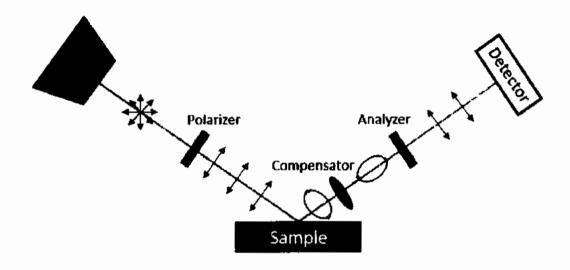


Fig. 4.10: Schematic spectroscopic ellipsometry setup [66]

As shown in Figure 4.9, a light beam is thrown on sample by light source. Light beam reflected back of the sample. This light beam is then analyzed to see what sample did to this light beam. Information is extracted from this light beam. Information like phase difference (delta Δ), amplitude ratio (psi, Ψ) and thickness of sample can be calculated [75].

Mathematical calculation of SE is given below.

Reflection:

$$\emptyset_i = \emptyset_r \tag{4.23}$$

Refraction:

$$n_1 \sin \emptyset_1 = n_2 \sin \emptyset_2 \tag{4.24}$$

Delta:

$$\Delta = \delta_1 - \delta_2 \tag{4.25}$$

Where δ_1 and δ_2 are phase difference. Ranges are from 0 to 360°.

Psi:

$$\tan \Psi = \frac{|R^p|}{|R^s|} \tag{4.26}$$

Ranges are from 0 to 90°.

Fundamental Equations of Ellipsometry:

$$\rho = \frac{R^p}{R^s} \tag{4.27}$$

$$\rho = \tan \Psi \, e^{j\Delta} \tag{4.28}$$

$$\tan \Psi e^{j\Delta} = \frac{|R^p|}{|R^s|} \tag{4.29}$$

4.8.2 Photoluminescence spectroscopy

Photoluminescence spectroscopy (PL) is optical measurement technique which is nondestructive and non-contact probing method. In this process, light beam or photons are directed on to the sample, sample absorbed this energy and a process occur which called photo excitation. In photo excitation process, materials atoms absorb light and jump into higher electronic energy level. Then, they release energy (photon) and come back to lower energy level. The emission of light/photon is known as luminescence and this process is called photoluminescence [76] as shown in Figure 4.11.

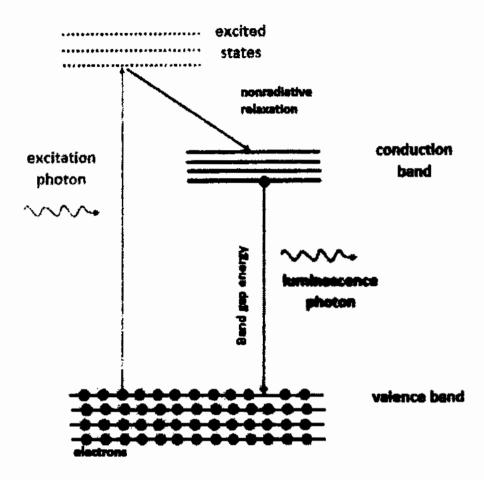


Fig. 4.11: Photoluminescence process [76]

Photoluminescence spectroscopy (PL) uses laser beam to capture light which is generated from substrate (Luminescence photons). By analyzing and measuring this luminescence spectrum, following calculation can be measured.

- · Band gap
- Recombination mechanism
- Impurity level
- Material quality
- Molecular structure
- Molecular crystallinity
- Defect detection

4.8.3 Classification of photoluminescence

The phenomenon of photoluminescence in semiconducting material either intrinsic or extrinsic is based on the electronic transition inside the material. The type and principle of both intrinsic and extrinsic photoluminescence is discussed in the subsequent section below:

4.8.3.1 Intrinsic photoluminescence

Intrinsically this phenomenon occurs in semiconductor material in three ways (1) excitonic emission (2) band to band and (3) cross luminescence

Exciton luminescence: This type of luminescence occurs inside a solid material when and excited electron recombine with a hole. These excitons are further classified in to the Wanniermott and Frenkel based on their generation and recombination mechanism. The Wannier mott describes a columbic interaction between electron in conduction band and a hole in the valence band. This type of excitons is stable at low temperatures and occurs only in inorganic compounds [77].

The Frenkel model is true for those condition in which the lattice constant is greater the wavefunction of both electron-hole pair. This type of luminescence occurs only organic materials.

Band to band luminescence: This type of luminescence occurs when and exited electron from the conduction band recombine with a hole in the valence band at extremely high temperatures. Materials in which such type of luminescence phenomenon takes places includes Si, Ge and GaAs. Practical examples include bright laser in which band to band transition occurs in its pure form.

Cross-Luminescence: Cross luminescence occurs when an excited electron from the conduction band recombines which a hole generated in the outermost core of the valence band

and the energy of excitation is less than the band gap of the materials. Such phenomenon only occurs in BaF3, alkali and alkaline-earth halides and their double halides [77].

4.8.3.2 Extrinsic Luminescence

Extrinsic luminescence occurs inside a semiconductor material due to intentional or unintentional doping or defect densities. Such type of doping/defects may create a luminescence center and are called the activators and the material is knowns as phosphor. Extrinsic luminescence is further categorized into localized and un-localized. In localized form the transition of free carriers occurs in bound states while in un-localized form the electric dipole transition occurs between two states [77].

4.8.3.3 Analytical background of Photoluminescence

Intensity of transmitted light through a sample when a laser light hit a light

$$I_{t} = I_{0}e^{-\alpha t} \tag{4.30}$$

 $\alpha(cm^{\text{-}1})$ is called absorption coefficient and it is a function of wavelength λ

Band gap of a material can be calculated using the formula

$$E = h v = h \frac{c}{\lambda} \tag{4.31}$$

Equation for luminescence polarization

$$I_z - I_x / I_z + I_x$$
 (4.32)

while the Ix and Iz represent the intensity of emitted light in x and z direction.

The emission intensity is related to photon flux as

$$N_{e}(\lambda_{em}) = \eta N_{i}(\lambda_{exc}) \{1 - \exp[-\mu(\lambda exc)x]\}$$
 (4.33)

where $N_i(\lambda_{exc})$ is the no of incident photons with the corresponding absorption coefficient.

1

Photoluminescence lifetime can be calculated as

$$\frac{1}{\tau} = \frac{1}{\tau r} + \frac{1}{\tau} + exp - \frac{\Delta E}{kT} + 1/\tau_Q \tag{4.34}$$

Where $(1/\tau_0)\exp(-\Delta E/kT)$ is the probability of electron at exited state at a given temperature T [78].

Chapter 5

Experiments, Results and Discussion

In this chapter we will discuss the electrical isolation of two photonically active integrated platforms i.e. GaN and InGaAsP, in detail. For their subsequent analysis, we have sub-divided this chapter into GaN and InGaAsP based studies which provides detailed analysis of respective counterpart.

5.1 Electrical Isolation of GaN based Matrix for PICs

GaN based Photonic Integrated Circuits (PICs) have now become a global contender for their wide range of applications owing to their physical characteristics. The GaN material system acts as a promising platform, compatible with silicon and sapphire substrates. Both the carrier transport and carrier removal techniques are vital to develop the efficient platform for the integration of photonic circuits.

For specifically GaN PIC perspectives, we have mapped the detailed analysis on the carrier removal techniques. For this we have chosen ion irradiation techniques for inter and intra device isolation within the common GaN based photonic platform. To achieve this metrology, we have chosen He⁺ and C⁺ ions to isolate active region in the photonic platform. In order to see the real extent of said carrier isolation, we have initially modelled the ion distribution using SRIM/TRIM software packages and studied the modeling based physical damage in terms of vacancies created by the incoming ion displacements at a particular depth of GaN platform. Physical ion implantations of subject ions are irradiated by real Ion implantation routines. After these routines we have mapped the carrier removal phenomena, by using detailed electrical analysis.

5.1.1 Device Simulation

For modeling and simulation point of view the initial sketch and localized volumetric region is needed where the device's integral parts may bombard with highly energetic ions and their impact onto the said GaN platform has studied in detail.

Initially the n-GaN matrix shown in Fig. 5.1 was simulated in Monte Carlo based computer code, namely, Stopping and Ranges of Ions in Matter (SRIM) [79]. The software predicts the ion placement into the device under test with specific dose and ion energy. The ion distribution and vacancy (density profiles) within the device matrix are shown in Fig. 5.2 for He⁺ dose of 1×10^{14} cm⁻² at 800 keV and C⁺ dose of 1×10^{14} cm⁻² at multi-energies of 800 keV, 1200 keV and 2500keV; respectively.

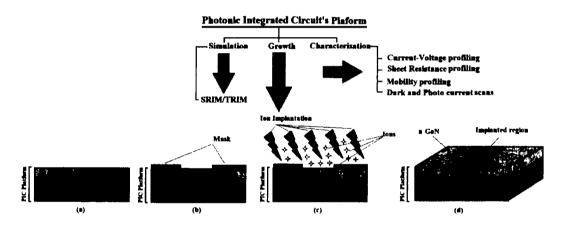
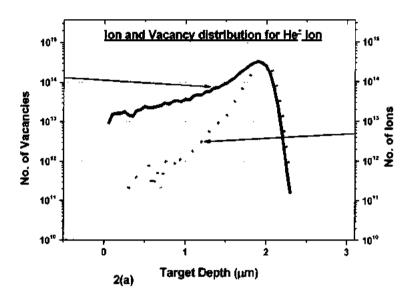


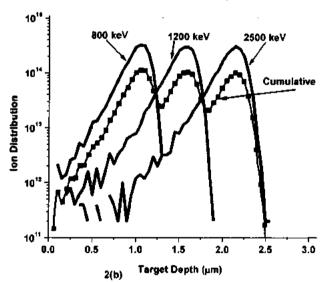
Fig. 5.1: Block diagram and Device schematic

The energy schedules were intentionally selected in such a manner to map the damage extent to same depth within the device structure. Normally, implant isolation is achieved by employing damage induced deep levels and chemical induced deep levels. For this matter we have employed He⁺ ion which would create damage related isolation and for C⁺ ion which may also cause mainly the chemical induced isolation. The vacancy and ion distribution profile are another important factor that may critically contribute to the damage related isolation and chemical related isolation respectively within the device matrix. The average vacancies and ion profiles with respect to the depth into the device for both the cases are presented in Fig. 5.2. C⁺

ion shows greater vacancy profile as compared to He⁺ one. This may be due to the heavier mass and physical volume of C⁺ ion, however He⁺ ion have greater penetration with respect to C⁺. The straggles associated with the projected ranges in each case at every implant energy used are within the acceptable limits for our design requirements.



Ion Distribution of C Ion in GaN with 800 keV, 1200 keV and 2500 keV



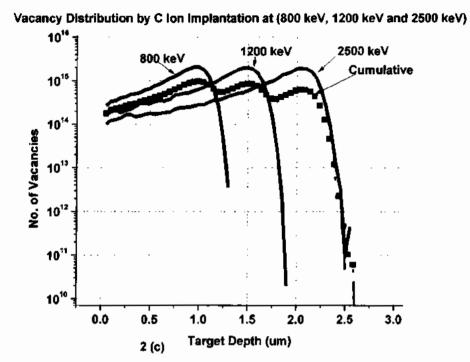


Fig. 5.2: Ion distribution and Vacancy Profiles (a) He⁺ Ion distribution and Vacancy profile, (b) C⁺ Ion distribution (c) C⁺ Vacancy profile

5.1.2 Device Synthesis and Fabrication

To achieve inter and intra device isolation on PICs platform, physical implant schemes are adopted. For this 5 MV pelletron tandem accelerator (5 UDH-2-NEC) was used at National Centre for Physics, Islamabad. Implantation routines are performed on n-type GaN device (Sidoped with ~10¹⁹ cm⁻³) grown on to c-plane both sided polished sapphire's substrate. The initial thickness of n-GaN was about 5μm with Ga-faced polarity. Before ion implantation, samples of size 1 cm x 1 cm were cleaved from the parent wafer and cleaned with standard recipe. The multi-implant C⁺ and He⁺ samples were treated at different devices in each case. The schematic pictorial of overall experimental process and sample's geometry is shown in Fig. 5.1.

5.1.3 Device Characterization

For electrical and electro-optical characterization, I-V metrology system, Hall Effect SWIN-8800 and ASMEC was utilized whereas for post-implant annealing was performed on Rapid Thermal Processor (GSL-1500X-50RTP).

5.1.3.1 Current-Voltage Measurements

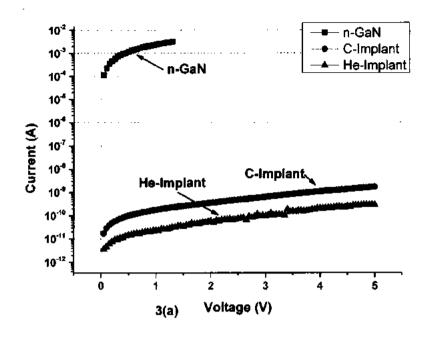
Based on the simulation results, one may predict the closest placement of ions within the device matrix that may be used for the electrical isolation due to the larger extent of physical damage into the device structure. For both the cases larger possibility exists to damage the host and to achieve implant driven carrier isolation phenomena. To gauge the maximum damage into the host lattice we have adopted multi-implant strategy for C⁺ (ion) case so that a probable larger number of vacancies are available within the device matrix. For He⁺ case, out of the simulated data, a single energy of 800 keV with a dose of 1x10¹⁴ cm⁻² was chosen. For both implant cases ion irradiation was performed at a specific region within the device structure with the unwanted area duly capped (refer to Fig. 5.1) in order to isolate two conductive regions which otherwise are electrically and optically active. The implant parameters for subject isolation schemes are shown in Table 5.1.

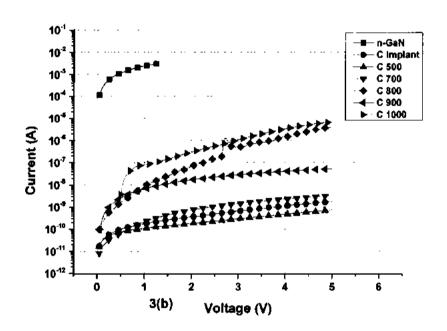
Table 5.1: Ion-Induced Isolation Schemes

	Impl	Implant specie	
Dopant Parameter	C ⁺ Ion	He ⁺ Ion	
	$-E_1 = 2500 \text{ keV}$		
Ion Energy	$-E_2 = 1200 \text{ keV}$	$- E_1 = 800 \text{ KeV}$	
	$-E_3 = 800 \text{ keV}$		
-	$- D_1 = 1 \times 10^{14} \text{cm}^{-2}$		
Dose	$- D_2 = 1 \times 10^{14} \text{cm}^{-2}$	- $D_1 = 1 \times 10^{14} \text{cm}^{-2}$	
	$- D_3 = 1 \times 10^{14} \text{cm}^{-2}$		

This is well established that by ion implantation, surface of host lattice may badly be damaged due to the inter and intra-atomic collisions [73]. As a result, the physical characteristics of device is likely to alter. After the physical ion implantation, the carrier transport properties, the extent of photo currents at different biased voltages and same characteristics at multiple annealing temperatures were investigated to gauge the extent and thermal stability of isolation characteristics. Fig. 5.3(a), 3(b) & 3(c) shows the two-point current-voltage characteristics of as implanted, annealed and host n-GaN device matrix.

The He⁺ as implant case shows lower current magnitudes as compared to multi-implant C⁺ cases. This lower current magnitude provides an insight that the extent of damage because of the He⁺ ion implantation is more than that of C⁺ implants. C⁺ being relatively heavier than He atoms may yield larger number of inter and intra-atomic collisions with specific kinetic energies, but its carrier removal rate may get influenced by its relatively higher electro negativity. After ion implantation the said samples was treated under rapid thermal annealing at 500°C for 60 seconds. At this temperature, the system contributes less current under given bias due to the possible higher magnitudes of electrical isolation achieved. As the annealing temperature increases further, the carrier removal/isolation capability of the said matrix goes on decreasing. This may be due to chemical nature of carbon atoms as known in some other works for GaN devices [80].





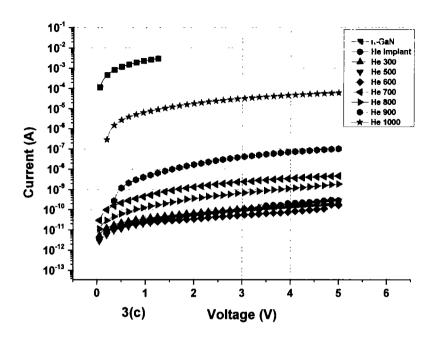


Fig. 5.3: Current-voltage characteristics of n-GaN, implant driven electrically isolated regions and post implant annealed devices (a) Comparison of n-GaN, He⁺ and C⁺ Ion implantation (b) C⁺ implantation region, (c) He⁺ implantation region

This may also be realized from Fig. 5.3(a-b) that the applied electric field also influences the current regimes in the device matrix (signature of the extent of damage occurrence within the lattice). For example in Fig. 5.3(b); for less than one-volt operating voltages (at 0.5 V), the current is in the tune of ~5.75x10⁻¹¹ A for samples annealed at 700°C, whereas the similar C⁺-implanted samples reflected around 3.65x10⁻⁹ A when subjected to 1000°C anneals and measured at 0.5V bias. At slightly higher operating voltages, for instance at 5V; the field tends to alter this trend. At 1000°C annealing temperature, C⁺ implanted devices show higher extent of leakage, which may be due to carbon atoms acted as chemical impurity with the host of the implant driven lattice damage recovery by virtue of annealing. There is a possibility of having both of the phenomena occurring at the same time.

Fig. 5.3(c) shows the Current-Voltage (I-V) characteristics of He⁺ implanted devices at different annealing temperatures. Likewise, C⁺ implant case, He⁺ irradiated case shows thermal stability at lower annealing temperatures (300-600°C) and enhances the isolation

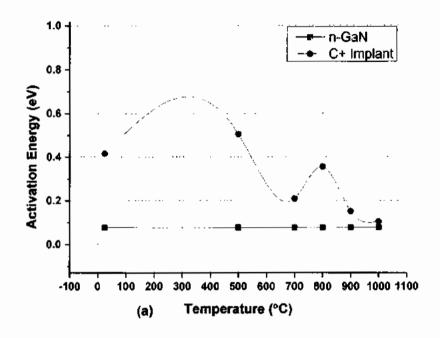
characteristics. The main advantage of He⁺ is its inert nature contributing to the damage alone events. At rather higher annealing temperatures, the charge flow from electrically isolated region tends to increase due to the larger extent of implant driven damage recovery. The charge flow in higher isolation regime approaches 1.7x10⁻¹⁰ A at 600°C and the extent of charge leakage increases up to 6.1x10⁻⁵ A at 1000°C. However, at higher annealing temperatures the trap density rapidly falls below the carrier concentrations and carriers returned to the respective conduction and valence band edges [81]. Although Carbon ion have higher mass than the He⁺ ions, but He⁺ ion shows ionic size hindrance effect, which is independent of the mass. This limitation explains why Carbon is not able to penetrate deeper into the lattice, even with multiple energy implants [82].

5.1.3.2 Current-Voltage based Arrhenius Analysis

Another parameter that may readily influence the isolation of the inter and intra device regions is the activation energy and governed by the (5.1) below:

$$\sigma_s = \sigma_o e^{\frac{Ea}{KT}} \tag{5.1}$$

Here ' σ_s ' the conductivity at temperature 'T', 'E_a' is the activation energy, 'K' is the Boltzmann's constant (=8.617x10⁻⁵ eVK⁻¹) and 'T' is the temperature in Kelvin. By linear approximation of (5.1), activation energies for all cases (reference device without implant and annealing; C⁺-implanted devices, He⁺-implanted devices and post implant annealed devices in both He⁺ and C⁺ cases) were calculated as shown in Fig. 5.4(a & b). The activation energy is the minimum energy needed to the carriers (available in the implant driven electrically isolated region) to conduct.



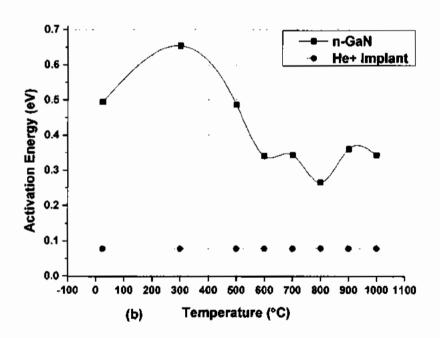


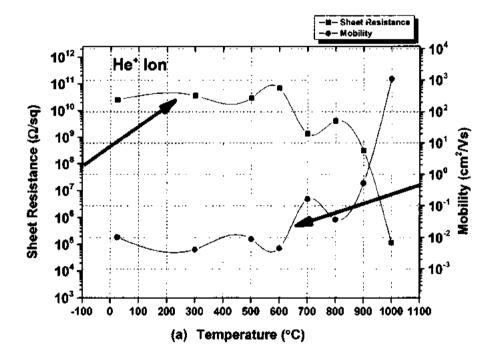
Fig. 5.4: Activation Energies of the process (a) C+ implanted region (b) He+ implanted region

Fig. 5.4 shows the trend of activation energies for He⁺ and C+ implanted devices and those which are annealed after implantation. The activation energy of parent Si doped GaN matrix was around 0.0776 eV, and 0.494 eV and 0.416 eV for an implanted He⁺ and C⁺ cases:

respectively. The higher magnitude of activation energy of He⁺ shows that larger physical damage was produced as compared to C⁺ implants. Thus, relatively higher energy is needed to conduct He⁺ implant region as compared to C⁺ isolated region. Consequently, less amount of charge carriers will flow from subject device stack.

5.1.3.3 Carrier dynamics of GaN Matrix

For both implant cases the initial thermal flux (300°C for He⁺ and 500°C for C⁺) enhances the isolation. For effective channel cases for electro-optical and photonic activity, less carriers and large amount of activation energy is required so that minimum leakage occurs from subject region. A general rule of thumb for achieving acceptable isolation in GaN device stacks is that the implanted region should have a sheet resistance in the tune of $10^7 \Omega/\text{sq}$ [83], [84], [85] & [86].



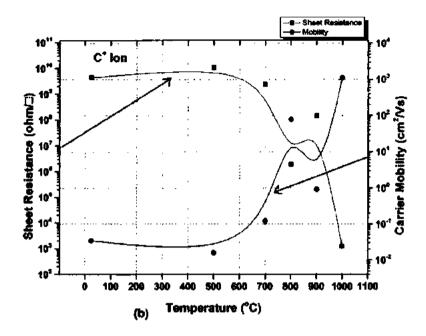


Fig. 5.5: Sheet Resistance and Carrier Mobility of implanted GaN matrix at multiple annealing temperatures (a)

He⁺Ion irradiation (b) C⁺Ion irradiation

Fig. 5.5 (a) & (b) shows the sheet resistance and sheet carrier mobility characteristics of all the devices implanted with C^+ and He^+ as well as those which were subsequently annealed. The sheet resistance of initial n-GaN over sapphire platform was measured as 16.9 Ω /sq. When this sample was irradiated with C^+ and He^+ implantation routines (separately), the sheet resistance increases 10^9 times as compared to the parent device. This was primarily thought to be due to defects formed because of the implantation assisted damage of the lattice. As a result of these traps, carriers removed from the bands contributed to significantly increase the sheet resistance [87]. The extent of damage, as shown in Fig. 5.5, produced from He^+ ion irradiation is larger as compared to C^+ implants.

For all annealed cases, the isolation achieved in the device matrix using He⁺ ion is deeper than the multi energy implant C⁺ case. Although the carbon multi energy implants produce large extent of physical damage in form of vacancies as compared to He⁺ (refer to vacancy profiles in Fig. 5.2), but the sheet resistivity of He⁺ ion cases is relatively higher. This may well be attributed to the chemical nature of Carbon atoms, confirming the results obtained in the I-V

analysis of these devices presented in Fig. 5.3. Carrier mobilities tend to follow the converse trend as compared to the sheet resistance in both the implant cases. The annealing dynamics seen to play a critical role in the recovery of damage in the lattice and consequently improving the conductivity (while reducing the extent of isolation achieved within the GaN-based PIC platform). This behavior is visible in both the device sets in case of He⁺ and C⁺ implants undergoing a progressively rising annealing temperature cycles.

5.1.3.4 Kinetics of dark and photo current

To inspect the photon driven carrier activation in GaN-based PIC platform, kinetics of electric current under dark and luminous condition at variable electric field was also performed. We have specially employed these measurements at zero applied bias, as well, to inspect the photo-induced charge voltaicity phenomena, for both the implant cases (He⁺ and C⁺ Implant).

During these measurements the samples were subjected initially under dark at a less than 200 lux intensity for 10 seconds and then subjected to luminous conditions at an intensity of about 179000 lux for next 10 seconds followed by another dark condition at 0 volt applied bias. As these measurements were performed under 0 volts applied bias thus the extent of larger current (during luminous condition) in both cases depicts that the photo-induced potential has developed that is contributing towards the higher magnitude of current. To gauge the photoconductive phenomena which is essential to address the free carrier loss mechanism in III-nitrides based PICs, we have performed same measurements under different bias conditions i.e. 1V-5V.

5.1.3.4.1 Kinetics of dark and photo current of He+ implanted GaN based PIC platform (As implanted and Annealed)

In this section, the case wise manipulation of He⁺ implanted n-GaN based Matrix for PICs has been discussed in detail. We have made all the measurements under different biased conditions i.e., from 0V (absence of bias) to 5V. All these measurements have been presented below in Figs. 5.6, 5.7, 5.8 and 5.9. These graphs provide an overview of the variation in dark and photo currents as He⁺ implanted sample have been annealed and subsequently measurements were carried out under different biasing conditions.

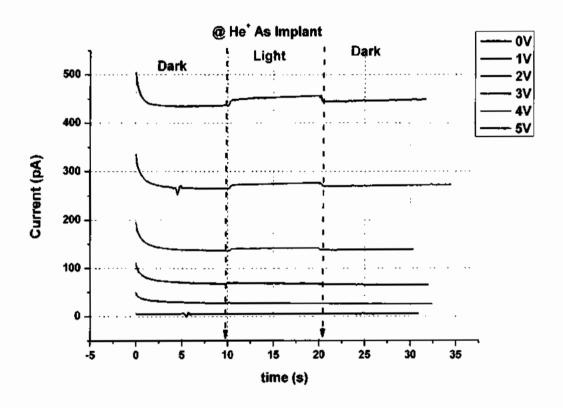


Fig. 5.6 Kinetics of Dark and Photo current for as He+ Implanted case

As can be seen clearly from above that maximum current and leakage current both are occurring for 5V drift.

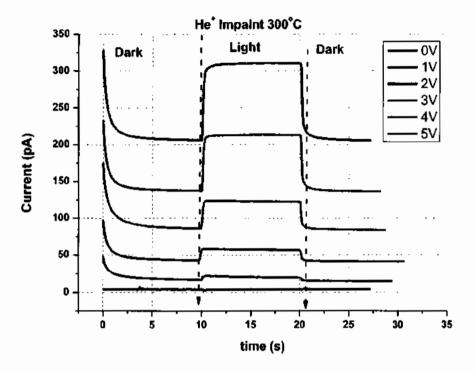


Fig. 5.7: Kinetics of Dark and Photo Currents for He⁺ Implanted annealed at 300°C

Here, an interesting observation is that magnitude of currents has been reduced from the as implanted case. This may point out to loss of carriers which were present in as implanted scenario and concurrent with our findings for Current-Voltage measurements as well.

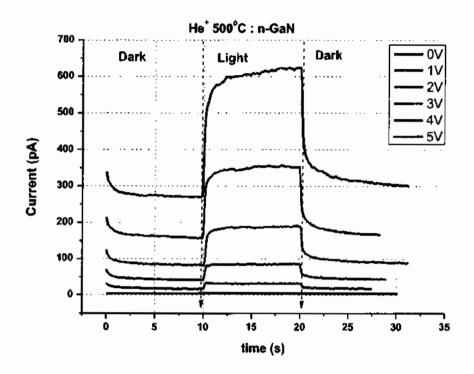


Fig 5.8: Kinetics of Dark and Photo Currents for He⁺ Implanted annealed at 500°C

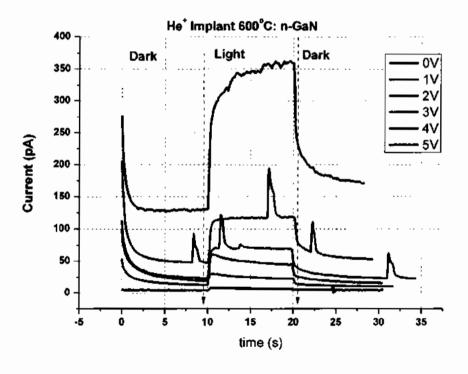


Fig. 5.9: Kinetics of Dark and Photo Currents for He⁺ Implanted annealed at 600°C

5.1.3.4.2 Effect of Annealing on Kinetics of Dark and Photo Current for He⁺ Implant

Here keeping the drift constant, the effect of annealing on the kinetics of dark and photo current have been elaborated. For this purpose, we have selected two biases i.e., 0V (absence of drift) and 5V (maximum drift). These effects have been clearly elaborated in Figs.5.10 and 5.11 below.

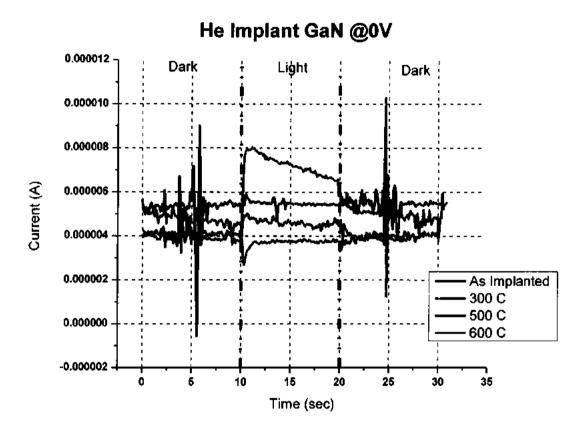


Fig. 5.10: Kinetics of Dark and Photo current for He+ implanted GaN at 0V

An important observation, firstly magnitude of photo current has gone down with Annealing but however afterwards it has recovered, and significant increase has been observed this has happened in with both bias conditions.

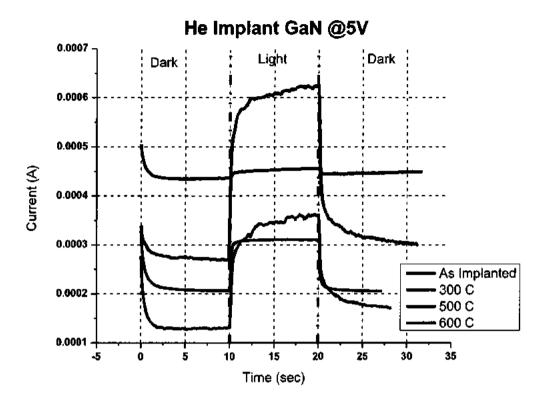


Fig. 5.11: Kinetics of Dark and Photo current for He⁺ implanted GaN at 5V

5.1.3.4.3 Kinetics of dark and photo current of C+ implanted GaN based PIC platform (As Implanted and Annealed)

In this section, the case wise manipulation of C⁺ implanted n-GaN based Matrix for PICs has been discussed in detail. We have made all the measurements under different biased conditions i.e., from 0V (absence of bias) to 5V. All these measurements have been presented below in Figs. 5.12, 5.13, 5.14 and 5.15. These graphs provide an overview of the variation in dark and photo currents as C⁺ implanted sample have been annealed and subsequently measurements were carried out under different biasing conditions.

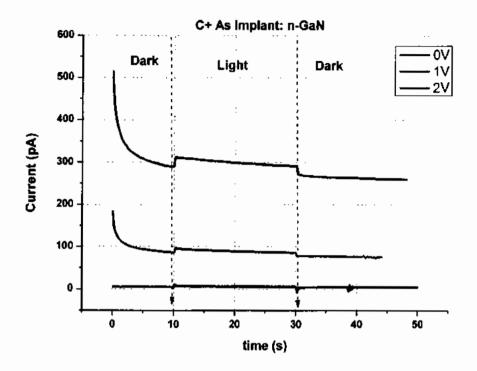


Fig. 5.12 Kinetics of Dark and Photo current for as C+ Implanted case

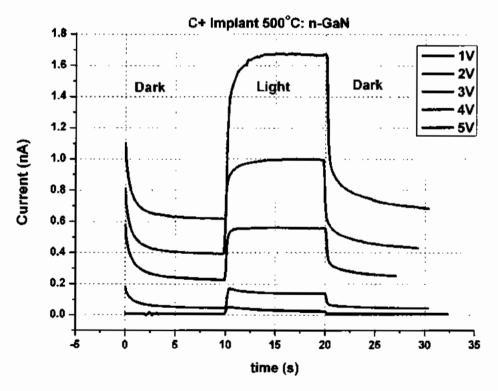


Fig. 5.13: Kinetics of Dark and Photo Currents for C* Implanted annealed at 500°C

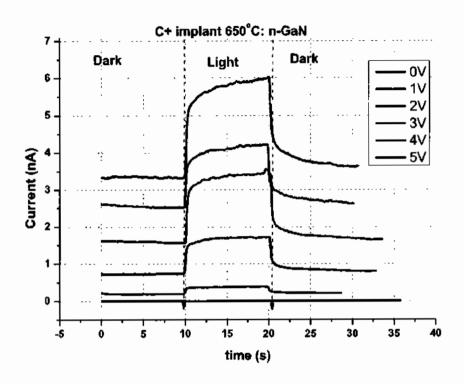


Fig 5.14: Kinetics of Dark and Photo Currents for C+ Implanted annealed at 650°C

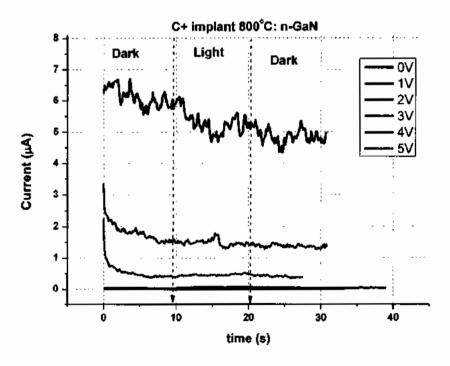


Fig. 5.15: Kinetics of Dark and Photo Currents for C+ Implanted annealed at 800°C

5.1.3.4.4 Effect of Annealing on Kinetics of Dark and Photo Current for C+ Implant

Here keeping the drift constant, the effect of annealing on the kinetics of dark and photo current have been elaborated. For this purpose, we have selected two biases i.e., 0V (absence of drift) and 5V (maximum drift). These effects have been clearly elaborated in Figs.5.16 and 5.17 below.

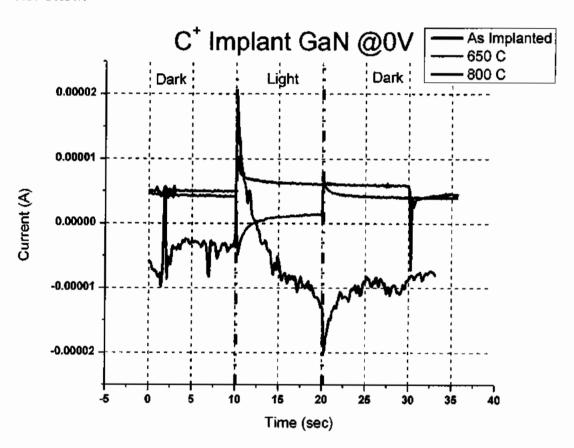


Fig. 5.16 Kinetics of Dark and Photo current for C+ implanted GaN at 0V

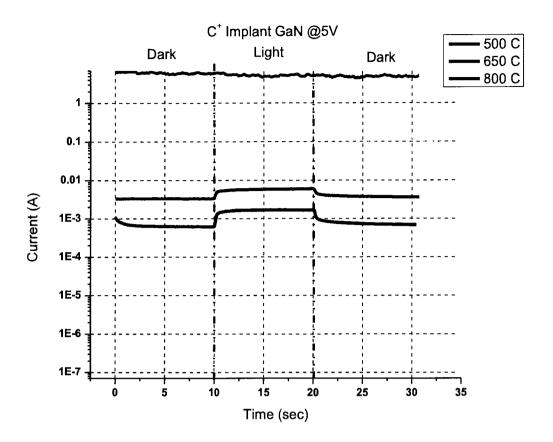


Fig. 5.17 Kinetics of Dark and Photo current for C⁺ implanted GaN at 5V

Clearly, there is a constant increase in conductivity of the sample as annealing temperature is increased. This points out to the important fact that as the damage caused by initial ion implantation recovers, the number of carriers available for conduction increases.

This can be noticed from both the as-implant cases that there is hardly any photo response observed. This may be due to the larger extent of physical damage which has prevailed after implantation, confirming the presence of an isolated region. As soon as these implanted samples are treated with thermal flux, they become activated and such physical region can be used as photonic node (transmitter). The exact values of dark and luminous currents under different bias conditions achieved after repetitive measurements are reported in tables 5.2 and 5.3 for, He and C ions respectively. These are the magnitudes of dark and photo currents under multiple biased conditions for 0V and 5V bias regimes under fixed optical power. From these

two tables one may clearly see that how much current been increased by incident photons at a particular implanted region.

Table 5.2: Dark and photo current under different bias conditions for He Ion Implant

Sample	@0V		@1V		@2V		@3V		@4V		@5V	
	Dark Current (A)	Light Current (A)										
He+- imp	-	-	2.7x10 ⁻	2.8x10 ⁻¹¹	6 7x10 ⁻¹¹	6.9x10 ⁻	1.3x10 ⁻¹⁰	1.4x10 ⁻¹⁰	2.6x10 ⁻¹⁰	2.7x10 ⁻¹⁰	4 3x10	4 5x10 ⁻¹⁰
He ⁺ 300	3.8x10 ⁻¹²	2.6x10 ⁻¹²	1.6x10 ⁻	2.2x10 ⁻¹¹	4.3x10 ⁻¹¹	5.8x10 ⁻	8.6x10 ⁻¹¹	1.2×10 ⁻¹⁰	1.4×10 ⁻¹⁰	2.1x10 ⁻¹⁰	2 1x10 ⁻	3 1x10 ⁻¹⁰
He ⁺ 500	3.8x10 ⁻¹²	5.0x10 ⁻¹²	1.7x10 ⁻	3.4x10 ⁻¹¹	4.1x10 ⁻¹¹	8.5x10 ⁻	8.2×10 ⁻¹¹	1.9x10 ⁻¹⁰	1.6x10 ⁻¹⁰	3 6x10 ⁻¹⁰	2.7x10 ⁻	6.2x10 ⁻¹⁰
He ⁺ 600	4.4x10 ⁻¹²	8.0x10 ⁻¹²	1.3x10 ⁻	3.0x10 ⁻¹¹	1.9x10 ⁻¹¹	6.0x10 ⁻	2 3x10 ⁻¹¹	1.2x10 ⁻¹⁰	4.9x10 ⁻¹¹	1 9x10 ⁻¹⁰	1.3×10 ⁻	3.6x10 ⁻¹⁰

Table 5.3: Dark and photo current under different bias conditions for C Ion Implant

Sample	@0V		@1V		@2V		@3V		@4V		@5V	
	Dark Current (A)	Light Current (A)										
C+-imp	4.9x10 ⁻	1.0x10 ⁻¹¹	8.6x10 ⁻	9.7x10 ⁻¹¹	-	-	-	-	-	-	2.9x10 ⁻	3.1x10 ⁻¹⁰
C+ 500	-	-	6.3x10 ⁻	4.9x10 ⁻¹¹	4.4x10 ⁻¹¹	1.7x10 ⁻	2.3x10 ⁻¹⁰	5.6x10 ⁻¹⁰	3 9x10 ⁻¹⁰	1x10 ⁻⁹	6.2x10 ⁻	1 7x10 ⁻⁹
C+ 650	4.2x10 ⁻	-4.8x10 ⁻	1.9x10 ⁻	3.9x10 ⁻¹⁰	7.3x10 ⁻¹⁰	1.7x10 ⁻⁹	1.6x10 ⁻⁹	3 6×10 ⁻⁹	2.5x10 ⁻⁹	4.2x10 ⁻⁹	3.3x10 ⁻⁹	6.0x10 ⁻⁹
C+ 800	5.6x10 ⁻	1.2x10 ⁻¹¹	5.0x10 ⁻⁹	1.4x10 ⁻⁸	2.6x10-8	7x10-4	-	-	-	-	-	-

5.1.3.5 Charge Transient Analysis of GaN based PIC platform

Another diagnostic on atomistic scale is performed in order to observe the migration of induced trapped charges by the drift pump mechanism providing an insight to the electronic defects or trapping centers. The influence of light and field on these centers will be of importance on device level when intra-device isolation is desirable to achieve on PIC's substrate. A Charge based Deep Level Transient Spectroscopy (Q-DLTS) has been performed on both the implant cases, in order to study the impact of trap levels placed within the energy band picture and its associated characteristics that may be generated by the migration process of alien ion species.

Q-DLTS is actually charge relaxation technique that provides an insight of the concentration, capture cross-section and energy of trap levels/defects placed in the near premises of conduction and valance band edges. Measured spectra of Q-DLTS is between the independent variable of rate window ' τ '. This is a function of the precisely proportional decay times of device's initial discharge time i.e. t_1 and final discharge time i.e. t_2 . For thumb calculations, these times should be perfectly proportional i.e., ratio $t_1/t_2 = \alpha$ and the rate window ' τ_m ' is related in Equation 5.3 as [73] & [88]:

$$\tau = \frac{t_2 - t_1}{\ln(\alpha)} \tag{5.3}$$

The discharging charges Q₁ and Q₂, during discharge times of t₁ and t₂ are related in Equation 5.4-5 as:

$$Q_1 = Q_0 \exp(-e_n t_1) (5.4)$$

$$Q_2 = Q_0 \exp(-e_n t_2) (5.5)$$

As Q-DLTS measures the change in charge magnitude as function of rate window ' τ ', thus, the difference in charge magnitude would be related in Equation 5.6 as:

$$\Delta Q = Q_2 - Q_1 \tag{5.6}$$

Which can be further related as in Equation 5.7 below:

$$\Delta Q = Q_0 [\exp(-e_n t_2 - \exp(-e_n t_1))]$$
 (5.7)

Where, ' e_n ' is the electron emission rate and quantitative expression has been given in Equation 5.8 below:

$$e_n = \sigma T_n T^2 \exp(-\frac{E_T}{KT}) \tag{5.8}$$

Where ' σ ' is the capture cross section, 'T' is the temperature in Kelvin, ' E_T ' is the trap's (activation) energy, 'K' is the Boltzmann constant, and ' T_n ' is defined in mathematical terms as in Equation 5.9 below [73], [88], [89], [90]

$$T_n = 2(3)^{\frac{1}{2}} \left(\frac{2\pi}{h^2}\right)^{\frac{3}{2}} k^2 m_n \tag{5.9}$$

Where, 'h' in equation above is Planck's constant and ' m_n ' is the effective mass of an electron. Another trap parameter is ' N_T ' i.e. trap concentration/density which can be calculated from Equation 5.10 below:

$$N_T = \frac{4\Delta Q_{max}}{qA} \tag{5.10}$$

Where, 'q' is universal charge constant (=1.69x10⁻¹⁹C), 'A' is two-dimensional area of physical contact (where charge accumulates two-dimensionally just at the interface of GaN/Al₂O₃ and metallic contact) and ΔQ_{max} is the maximum change in charge magnitude that may observed during the entire recording cycle by a specialized charge collecting circuit.

A detailed analysis of Charge transients has performed in order to observe the migration of induced trapped charges by the drift pump mechanism providing an insight to the electronic defects or trapping centers. The influence of light and field on these centers will be of importance on device level when intra-device isolation is desirable to achieve on PIC's substrate. A Charge based Deep Level Transient Spectroscopy (Q-DLTS) has been performed on both the implant cases, in order to study the impact of trap levels placed within the energy band picture and its associated characteristics that may be generated by the migration process of alien ion species.

Q-DLTS characterizations are initially done at a fixed voltage level for a definite period of time, just to synchronize the power supply and device under test (we have sustained this drift level at about 0V) and then the external bias was increased to a particular level by which one needs to lift off the bias of ~3000mV for the entire charging time of ~100ms. This is mainly, the time (charge time) at which the ion assisted traps of parent lattice i.e. InGaAsP are somehow filled completely at 3000mV. After the trap's charge time (~100ms) when an external 3000mV biased was removed, the natural discharge mechanism might provoke and would be considered into accounts mainly. Thus, the drift driven voltage (discharge) assisted charge-level continuously decreases from maximum (Qo) to theoretically zero level [73], [89], [90] & [91]. This discharge time (between 3000mV - Zero volts) may vary from case to case, this may be decided by an internally damaged GaN's lattice nodes that eventually causes the traps and play directly here with due to the effective RC (Resistance-Capacitance) coupled parasitic nature of voids and interstitials of said damaged lattice. This specialized nature may directly influence the electro-optical characteristics of said matrix because of the ions implanted carrier dynamics, which may well be exploited to fabricate the substrates for PIC's. The experimental approach along with their associated timings of charge-discharge nature of subject ion-assisted voids/interstitials of InGaAsP is shown in Figure 5.18.

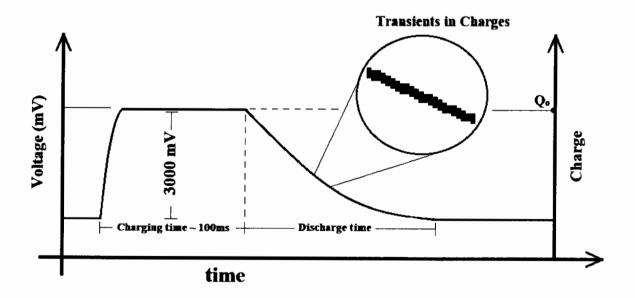
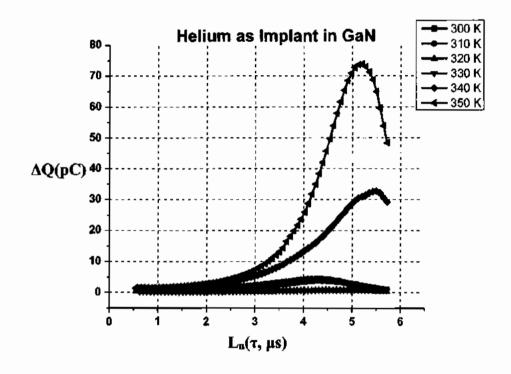


Fig. 5.18: Instrumentational approach towards charging-discharging of ion-assisted InGaAsP traps

During this time (discharge event) charge collected by the trap centers was released and recorded between multi-time intervals with equal initial and final discharge times of t_1 and t_2 as referred in Equation 3 and 4. The physical importance of trap centers and their associated parameters i.e. Trap concentration (N_T), Trap Energy (E_A commonly referred as E_T) and capture cross-sections(σ) were explained, at length, in our previous work [73], [89] & [90].

5.1.3.5.1 Charge Transient Analysis for He⁺ Implanted GaN based PIC Platform (As Implanted and Annealed)

In order to investigate the trap parameters i.e., trap densities (N_T), Capture cross section (σ), and trap level energy (E_T); The charge transient analysis of He⁺ implanted n-GaN matrix has been characterized. For all annealed He⁺ implanted samples; the samples were measured at 300K, 310K, 320K, 330K, 340K and 350K ambient temperatures and by linear approximation of Equation 5.8 (also called Arrhenius analysis), the trap energy (E_a) and capture cross section have been calculated. For trap concentration Equation 5.10 has been used. These analyses have been presented in Figs. 5.19, 5.20, 5.21 and 5.22. From subject analysis one have calculated the trap level energy and capture cross section of GaN based He⁺ implanted PIC platforms. The activation energy and capture cross section of as- implanted, 300°C, 500°C and 600°C are; Ec-0.5eV, 4.55x10⁻³⁴ cm²; Ec-0.4eV, 8.97x10⁻²³cm²; Ec-0.134eV, 1.68x10⁻²⁸cm² and Ev+0.004eV, 2.62x10⁻²⁶cm², respectively. Higher the capture cross section higher will be probability of concern trap which may capture the free charge carrier, thus, 500°C temperature is strong center that may capture maximum free carriers.



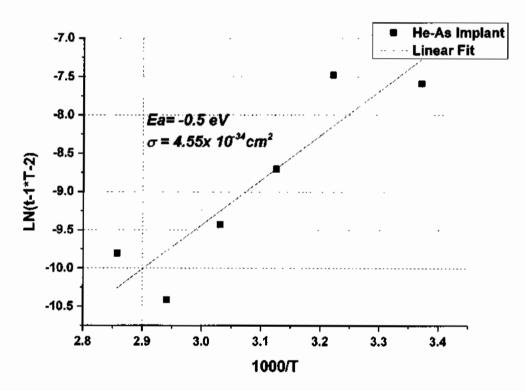


Fig. 5.19: Arrhenius Analysis of as Implant He* ion

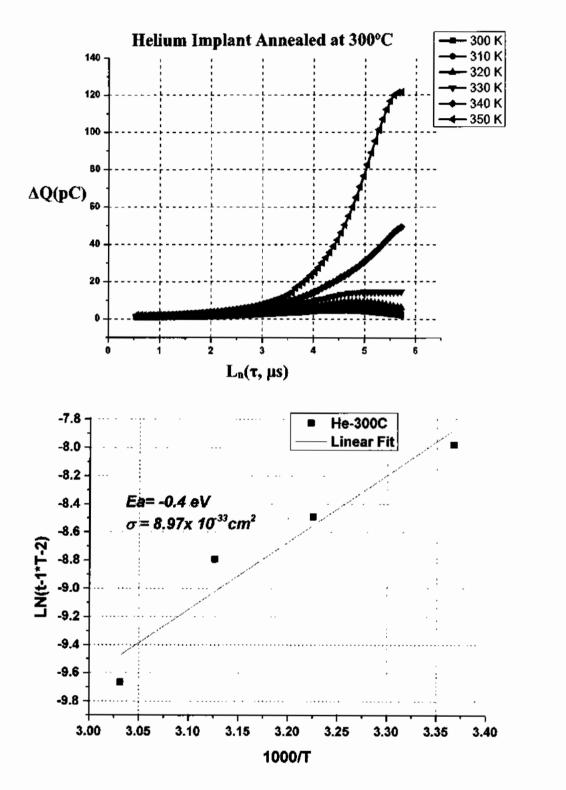


Fig. 5.20: Arrhenius Analysis of He+ implant annealed at 300°C

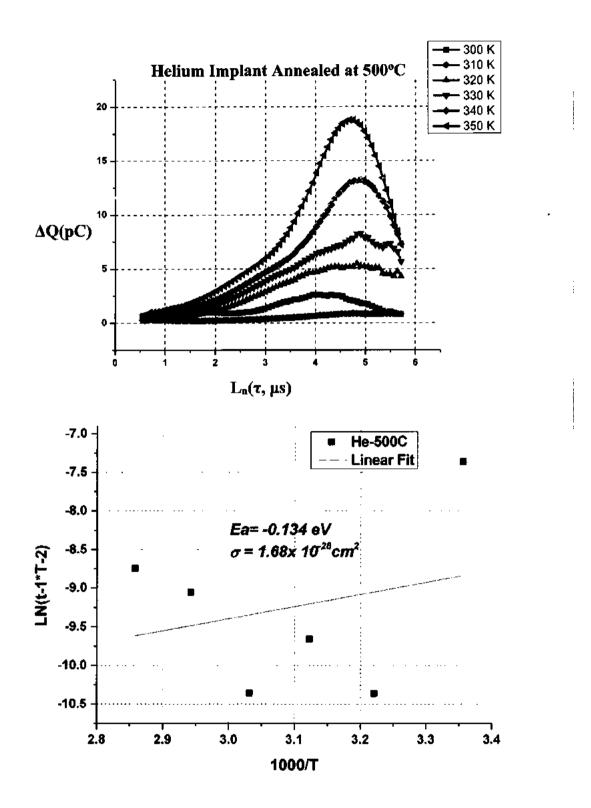


Fig. 5.21: Arrhenius Analysis of He⁺ implant annealed at 500°C

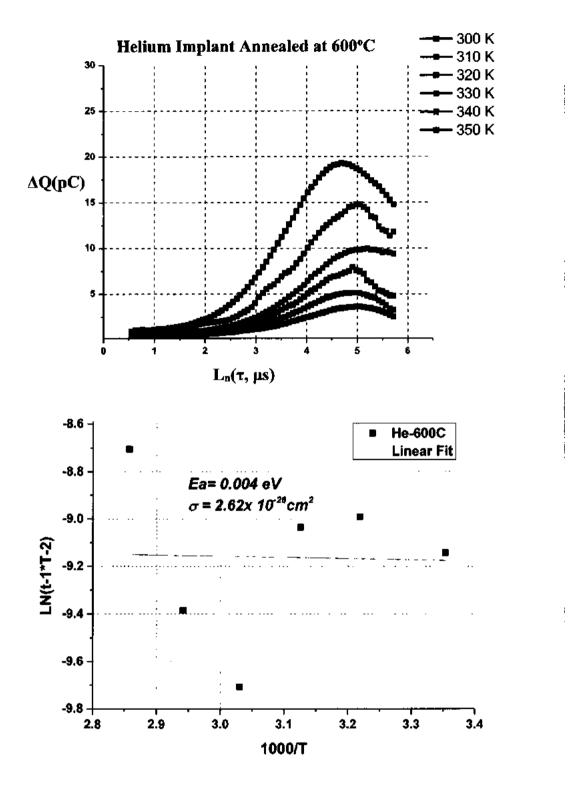


Fig. 5.22: Arrhenius Analysis of He⁺ implant annealed at 600°C

5.1.3.5.2 Charge Transient Analysis for C⁺ Implanted GaN based PIC Platform (As Implanted and Annealed)

In order to investigate the trap parameters i.e., trap densities (N_T), Capture cross section (σ), and trap level energy (E_T); The charge transient analysis of C⁺ implanted n-GaN matrix has been characterized. For all annealed C⁺ implanted samples; the samples were measured at 300K, 310K, 320K, 330K, 340K and 350K ambient temperatures and by linear approximation of Equation 5.8 (also called Arrhenius analysis), the trap energy (E_a) and capture cross section have been calculated. For trap concentration Equation 5.10 has been used. These analyses have been presented in Figs. 5.23, 5.24, 5.25 and 5.26. From subject analysis one has calculated the trap level energy and capture cross section of GaN based C⁺ implanted PIC platforms. The activation energy and capture cross section of as- implanted, 500°C, 650°C and 800°C are; Ec-0.321eV, 1.64x10⁻³¹ cm²; Ec-0.3eV, 1.37x10⁻²¹cm²; Ev+0.256eV, 2.31x10⁻²²cm² and Ev+0.009eV, 1.5x10⁻²⁴cm², respectively. Higher the capture cross section higher will be probability of concern trap which may capture the free charge carrier, thus, 650°C temperature is strong center that may capture maximum free carriers.

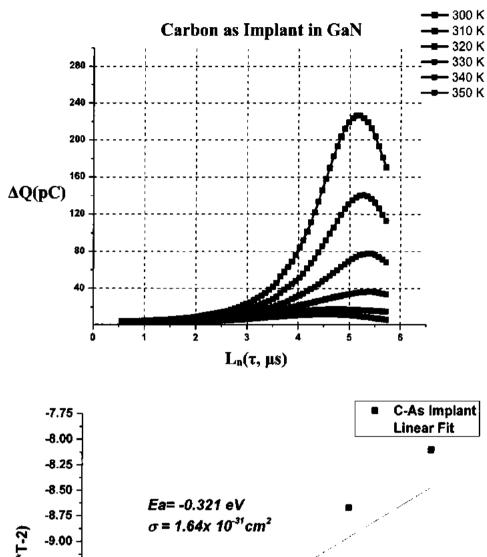


Fig. 5.23: Arrhenius Analysis of as Implant C+ ion

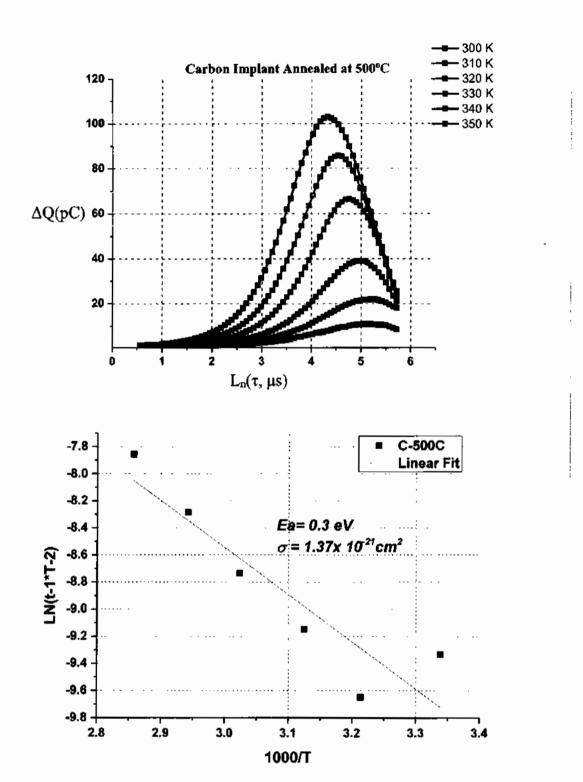


Fig. 5.24: Arrhenius Analysis of C* implant annealed at 500°C

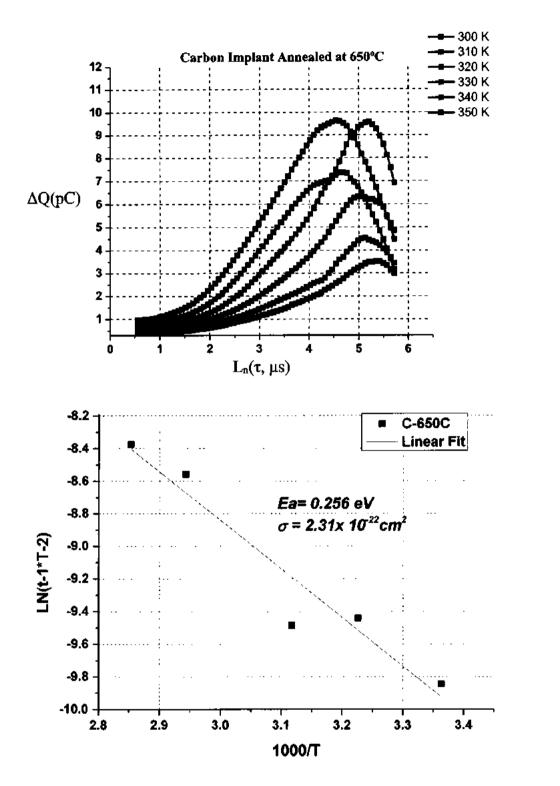


Fig. 5.25 Arrhenius Analysis of C⁺ implant annealed at 650°C

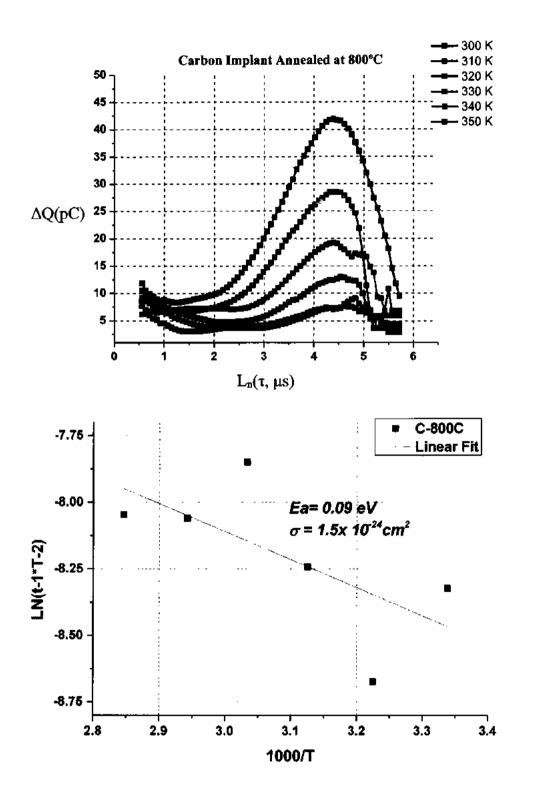


Fig. 5.26: Arrhenius Analysis of C+ implant annealed at 800°C

All the above results have been summarized in the Tables 5.4 and 5.5 below:

Table 5.4: Trap parameters for He⁺ Implant in n-GaN

Anne al. Temp			EA	σ				
	@ 300K	@ 310K	@ 320K	@ 330K	@ 340K	@ 350K	(eV)	(cm²)
As- Implan t	2.7 × 10 ¹⁰	3.3 × 10 ¹⁰	6.3 × 10 ⁹	8.2 × 10 ⁹	1.6 × 10 ¹¹	3.3 × 10 ¹¹	-0.50098	4.55 × 10 ⁻³⁴
300 ℃	3.6 × 10 ¹⁰	4.7 × 10 ¹⁰	6.7×10^{10}	1.1 × 10 ¹¹	-	-	-0.40979	8.97 × 10 ⁻³³
500 °C	2 × 10 ¹⁰	7.09 × 10 ⁹	4.25 × 10 ¹⁰	5.9 × 10 ¹⁰	845 × 10 ¹⁰	1.1 × 10 ¹¹	-0.13379	1.68 × 10 ⁻²⁸
600 °C	2.4 × 10 ¹⁰	3.3×10^{10}	4.59 × 10 ¹⁰	6.3 × 10 ¹⁰	9.26 × 10 ¹⁰	1.3 × 10 ¹¹	0.004461	2.62 × 10 ⁻²⁶

Table 5.5: Trap parameters for C+ Implant in n-GaN

Anne al. Temp				E _A	σ			
	@ 300K	@ 310K	@ 320K	@ 330K	@ 340K	@ 350K	(eV)	(cm ²)
As- Implan t	9.9 × 10 ¹⁰	1.4 × 10 ¹¹	2.3 × 10 ¹¹	3.9 × 10 ¹¹	6.7 × 10 ¹¹	1.1 × 10 ¹²	-0.32135	1.64 × 10 ⁻³¹
500 °C	6.6 × 10 ¹⁰	1.2 × 10 ¹¹	2.02 × 10 ¹¹	3.4 × 10 ¹¹	4.5 × 10 ¹¹	2.3 × 10 ¹¹	0.299009	1.37 × 10 ⁻²¹
650 ℃	2.5 × 10 ¹⁰	2.8 × 10 ¹⁰	4.1 × 10 ¹⁰	5.9 × 10 ¹⁰	5.5 × 10 ¹⁰	7.3 × 10 ¹⁰	0.256351	2.31 × 10 ²²
800 °C	8.1 × 10 ¹⁰	1 × 10 ¹¹	9.07 × 10 ¹⁰	1.6 × 10 ¹¹	2.03×10^{11}	3 × 10 ¹¹	0.09629	1.5×10^{-24}

5.1.3.5.3 Comparison of He⁺ and C⁺ Implants based on Charge Transient Analysis

In Figure 5.27, as per Equation (5.10), higher the ΔQ magnitude higher will be the trap densities/concentration i.e. $N_T \alpha \Delta Q_{max}$. From initial assessment (i.e. as-implant cases) as shown in Figure 5.27, the higher trap densities are present in C^+ case when relatively compared with its He⁺ counterpart. This phenomenon may readily be understood by the transmitted ions not from the lattice voids (vacancies profiles) because if the ions are part of the GaN's lattice

there is a higher probability to contribute during the conduction process. Thus, the impact of charged trap region in form of voids and interstitials due to ion-induced damage and provides an equivalent parasitic RC coupling on circuit level.

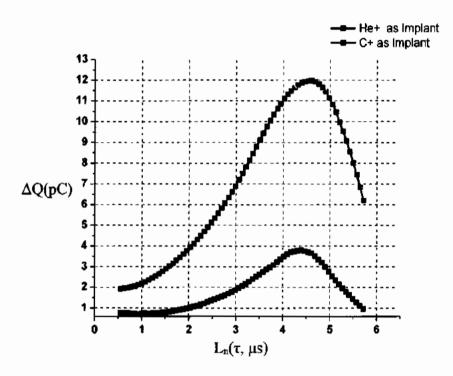
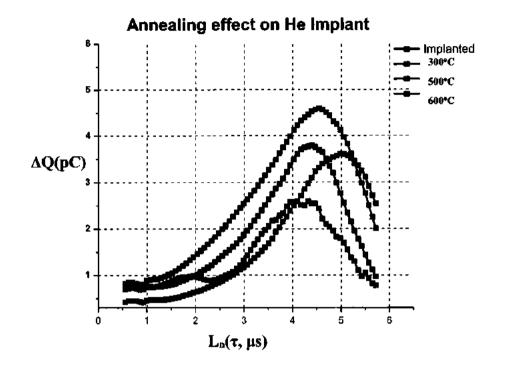


Fig. 5.27: Q-DLTS analysis of as-implant cases

For annealed samples of He⁺ and C⁺ implanted in GaN case wise transients have been shown in Figure 5.28 below:



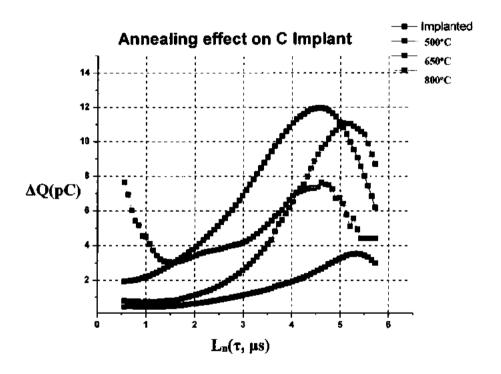


Fig. 5.28: Q-DLTS analysis of annealed cases

The surface trap concentrations of each such case has been calculated from Equation 5.10 and summarized in Table 5.4 and 5.5.

Other associated trap parameters that is determined from the linearization of Equation (5.8) are trap energy level (E_T) and the capture cross-section (σ). To evaluate both of these parameters, one may vary the temperature 'T' and scan the same spectra as shown in Fig.18. From this whole scan, the slope of the curve provides the information of trap location (E_T) and y-intercept directs the capture cross-section (σ). The sign of trap energy levels has much importance because this provides the information about the generation and recombination centers with-in the band gap i.e. negative signed trap (generation center) localized near to conduction band edge and positive signed trap (recombination center) localized near to the valence band edge. The self-explanatory energy band picture for both the implant cases along with their respective trap centers are shown in Figure 5.29.

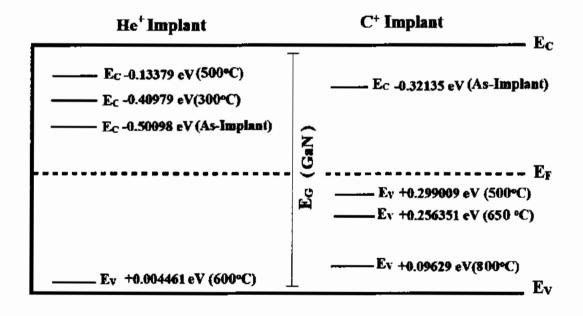


Fig. 5.29: Trap assisted energy band picture of GaN after the ion implantation and post processing annealing

5.1.3.6 Transient of Photo Voltage (TPV) Analysis of GaN based PIC Platform

The transient behavior of photo voltage (TPV) has also been studied where we have applied a sharp pulse of light to study the electro-optical behavior of all said devices. During this study, the anode and cathode both electrical contacts are placed at is zero volts. This specialized configuration has been adopted just to study the electrical response to gauge the optical drift mechanism of the GaN matrix. During this analysis are fixed intensity of the same optical resource has applied in order to generate electrical charge, during this phenomena the band gap of the expectation source is same, thus, the incoming energy of excited Photon has also been fixed. Now, it's up to the measurand sample that the band gap of said sample is higher or lower with respect to the incoming excited photons energy. When these photons strike with the zerodrift potential surface, the energy of photons transfers to the stroked lattice of the sample. During this process bounded Carriers of the lattice becomes free and collected at the anode and cathode of the sample and are measured. For zero-volt drift potential, these generated Carriers are produced only for a limited period of time commonly called transients. Upon these transient the developed voltage Rises to the steady state value and the decay of the Carriers be recorded as a function of time. When the sharp light ends up then the decay of the photo voltage may also be recorded, and this value decreases up to zero drift bias (i.e. initial condition of the pre-pulsed). Photo voltage transient at the end of the light pulse consists of rapid drop followed by the slower decay. The initial drop is due to electron-hole pair recombination and the slow decay is due to carrier emission [73].

For all said samples (He⁺ and C⁺); the optical illumination has applied and varied the drift electrical bias and scanned the photovoltage spectra.

5.1.3.6.1 TPV measurements for He⁺ Implanted GaN based PIC Platform (As Implanted and Annealed)

The TPV measurements of He⁺ implanted samples have been recorded for as implanted and annealed at 300°C, 500°C and 600°C at multiple drift bias, which has been varied from 0V to 5V. All the measured spectra are presented below in Figs. 5.30, 5.31, 5.32 and 5.33:

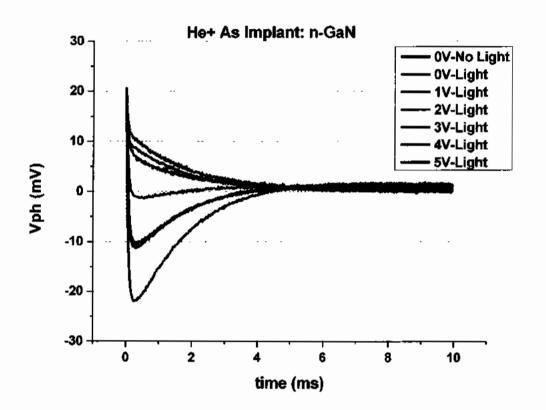


Fig. 5.30: Transient Photovoltage spectra for as Implanted He⁺ sample

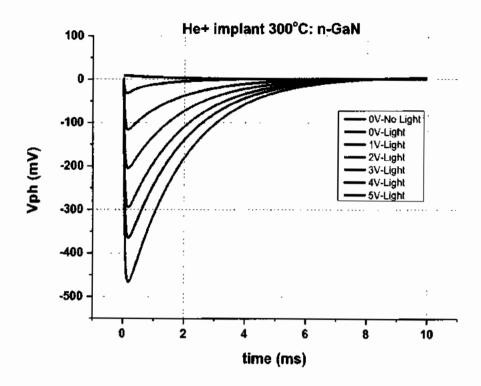


Fig. 5.31: Transient Photovoltage spectra for He+ Implanted annealed at 300°C

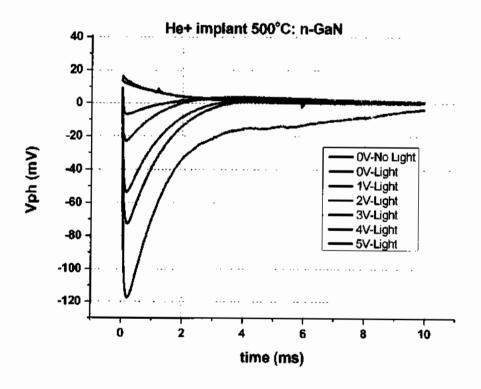


Fig. 5.32: Transient Photovoltage spectra for He⁺ Implanted annealed at 500°C

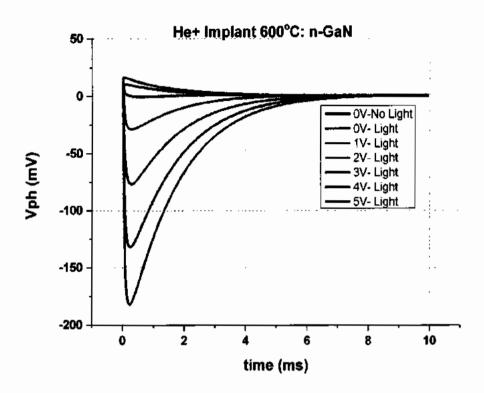


Fig. 5.33 Transient Photovoltage spectra for He⁺ Implanted annealed at 600°C

All the above-mentioned spectra clearly reflects a steady increase in photovoltage response in relation to increase in bias. This highlights the fact that more and more carriers are overcoming traps and contributing in current flow as electric field has been enhanced.

5.1.3.6.2 Conclusive: TPV measurements of He+ implanted GaN PIC

TPV measurements can also be used to highlight the importance of annealing process by keeping the bias constant and increasing the annealing temperature. This will reflect the amount of recovery that has occurred due to annealing. These comparative graphs (shown in Figure 5.34 and 5.35) can easily be generated by keeping the bias constant and reflecting the variation in spectra at different temperatures.

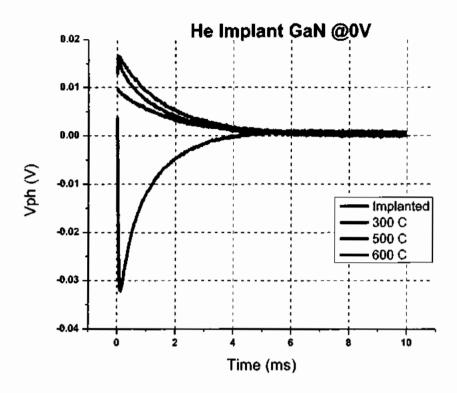


Fig. 5.34: Transient Photovoltage spectra for He+ Implanted keeping bias at 0V

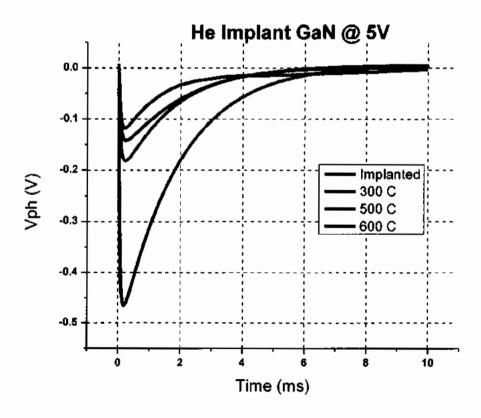


Fig. 5.35: Transient Photovoltage spectra for He⁺ Implanted keeping bias at 5V

5.1.3.6.3 TPV measurements for C⁺ Implanted GaN based PIC Platform (As Implanted and Annealed)

The TPV measurements of C⁺ implanted samples have been recorded for as implanted and annealed at 500°C, 650°C and 800°C at multiple drift bias, which has been varied from 0V to 5V. All the measured spectra are presented below in Figs. 5.36, 5.37, 5.38 and 5.39:

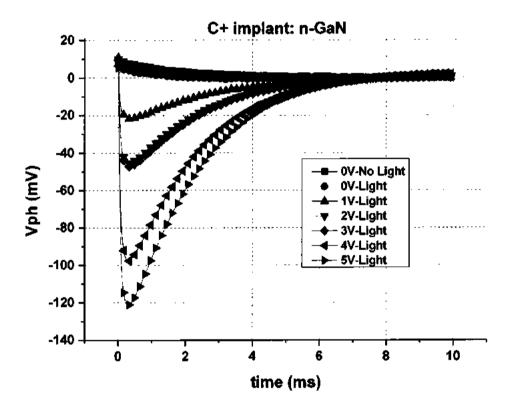


Fig. 5.36: Transient Photovoltage spectra for as Implanted C⁺ sample

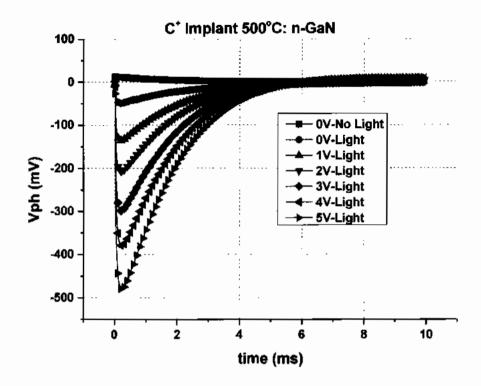


Fig. 5.37: Transient Photovoltage spectra for C⁺ Implanted annealed at 500°C

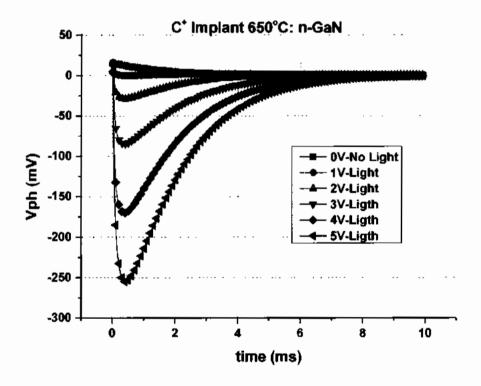


Fig. 5.38 Transient Photovoltage spectra for C* Implanted annealed at 650°C

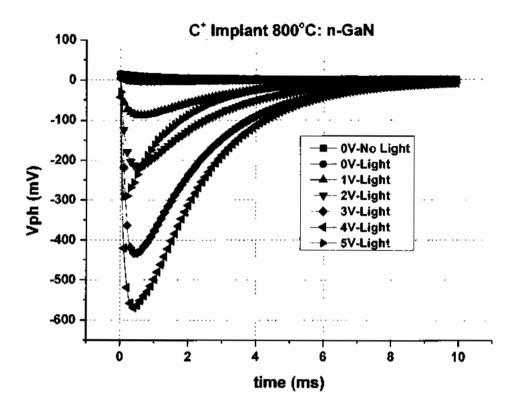


Fig. 5.39 Transient Photovoltage spectra for C+ Implanted annealed at 800°C

Spectra clearly reflects steady increase in response in relation to increase in bias. This highlights the fact that more and more carriers are overcoming traps and contributing in current flow as electric field has been enhanced.

5.1.3.6.4 Conclusive: TPV measurements of C+ implanted GaN PIC

TPV measurements can also be used to highlight the importance of annealing process by keeping the bias constant and increasing the annealing temperature. This will reflect the amount of recovery that has occurred due to annealing. These comparative graphs (5.40 and 5.41) can easily be generated by keeping the bias constant and reflecting the variation in spectra at different temperatures.

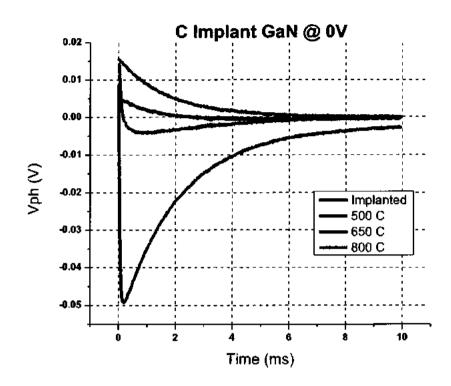


Fig. 5.40: Transient Photovoltage spectra for C+ Implanted keeping bias at 0V

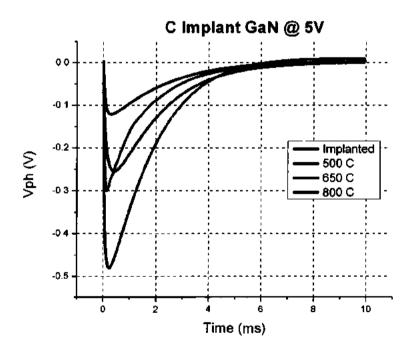


Fig. 5.41: Transient Photovoltage spectra for C+ Implanted keeping bias at 5V

5.2 Electrical Isolation of InGaAsP based Matrix for PICs

InGaAsP based technologies are more favorable due to its unique monolithic integrated nature. For an efficient electro-optical device structure, there is a keen interest to develop active and passive components to suffice the needs of monolithic platform. Thus, carrier's transport and removal regions are carefully fabricated with low optical and electronic signal loss in order to optimize the signal to noise ratio (SNR) to effectively produce monolithic chip. In this specialized study we have provided an insight about the effective multi-implant ion-assisted carrier removal capability of the highly conductive epitaxially grown InGaAsP/InP device matrix as PIC's substrate. For this multi-implant strategy has been adopted with C+ and Ni+ ions implanted separately. Their dosage's along with ion energies are simulated rigorously before the actual implantations. Post implant measurements of Sheet resistance, mobility, drift driven electric fields, current-voltage, Arrhenius based activation energies, charge based transient analysis and detailed investigations of traps have been performed to study the viability of carrier removal scheme for the stable as well as reversible electrical isolation of this photonic integrated circuit's platform. Trap parameters identified as a result of a specialized charge deep level transient spectroscopy provides an insight about the energy levels and possible evaluation of recombination/generation centres for effective photonic activity within the device regions. The optical loss study has been performed to inspect the optical hinderance levels into the said InGaAsP PIC matrix.

5.2.1 Device Simulation

In order to predict the actual ion placements through ion-implantation routine and their cumulative effect in terms of vacancy profile stopping and Range of Ions in Matter (SRIM) [79] software is used. We have chosen multi-energy implant routines in order to produce larger impact (in form of vacancies) that produce physical damage and contribute rather high

magnitude of lattice disorder and enhance the depletion of free carrier into the host InGaAsP lattice. For both ions (Ni⁺ and C⁺) used in this study, we have simulated multiple ion energies and dosages for ion distribution limited to the 1μm depth (because of the physical dimensional constraints of epi-layer of InGaAsP). For C⁺ case; the ion energies of about 800 keV (dosage of 1x10¹⁵cm⁻²) and 1000 keV (1x10¹³ cm⁻²) was chosen. Meanwhile, for separate Ni⁺ case; we have chosen 2000keV (1x10¹⁴cm⁻²) followed by 1000keV (1x10¹⁵cm⁻²) ion energies. The cumulative effect of each ion assisted energy on the InGaAsP device matrix is shown in Figures 5.42 and 5.43.

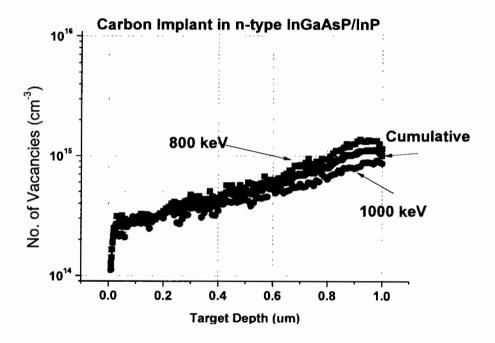


Fig. 5.42 Vacancy profile of C+ ion

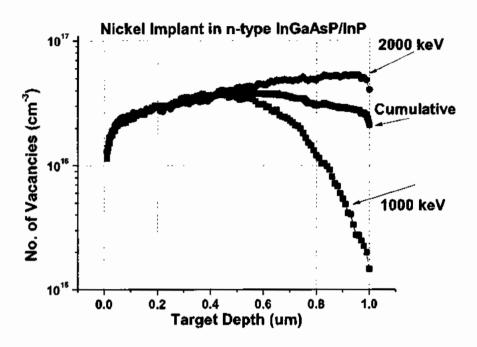


Fig. 5.43 Vacancy profile of Ni⁺ ion

Figures 5.42 and 5.43 provide an extent of vacancy profiles of both simulated ions. Also, the cumulative effect of the irradiation can also be visualized. Higher extent of vacancy generated by the Nickel ions is due to their higher mass which eventually produce greater momentum when striking through the host lattice. Thus, higher amount of damage may be observed for Ni⁺ case in comparison to C⁺ implantation. Table VI shows a summary of some important design parameters extracted from SRIM simulations for both the implant cases in n-type InGaAsP/InP device matrix.

Table 5.6 Monte Carlo based Simulated Results using SRIM

Parameter	Ca	rbon (C ⁺)	Nickel (Ni ⁺)		
	800 keV	1000 keV	1000 keV	2000 keV	
Average Projected Range (Å)	7734	7226	5799	7144	
Average Straggling (Å)	1841	2142	2061	2040	
Average Vacancy/Ion	665	480	11922	10899	
Total Backscattered Ions	21	26	46	22	
Total Transmitted Ions	8351	9451	200	7574	

One can observe that maximum vacancies are produced for both of Ni+ implant cases. Further; for both ion cases, the lower the energy, the higher will be the damage and vice versa. The straggles associated with the projected ions for each case are within the acceptable limits for our geometrical design of the device.

5.2.2 Device Synthesis and Fabrication

To inspect the carefully simulated ions of C^+ and Ni^+ , one must assess the behavior, stability and possibility for reversibility of the electrical isolations created in the active device regions. Initially, the undoped wafer of 350 μ m thick InP with <100> crystal orientation was epitaxially grown with heavily doped (n-type, ~10¹⁹cm⁻³) 1 μ m thick InGaAsP layer. The device was cleaved from the parent wafer into smaller two 0.5 x 0.5 cm2 device structures subjected to physical ion implantations. 5MV pelletron tandem accelerator (5-UDH-2-NEC) at National Centre for Physics (NCP), Islamabad, Pakistan was used for Ion Implantation. Simulated parameters of ion energies and doses were used for actual implantation performed at 7° of beam angle and room temperature.

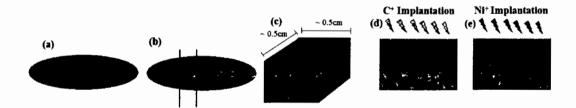


Fig. 5.44: InGaAsP device matrix, (a) InGaAsP/InP Wafer, (b) Cleaving of wafer into 0.5cm x 0.5cm, (c) Cross-sectional view of cleaved sample, (d) C⁺ Implantation, (e) Ni⁺ Implantation.

Figure 5.44 provides an overview of the process used i.e., (a) shows the InGaAsP/InP wafer, (b) shows the cleaving of said wafer, (c) shows the cross-sectional view of cleaved samples and (d-e) show the C+ and Ni+ Ion implantations, respectively.

In order to map the extent and influence of physical ion-implantations on subject matrix, the detailed transport and charge measurements were performed. For electrical characterization SWIN Hall-8800 and Automatic System for Material Electro-physical Characterization System (ASMEC) was used, Charge Deep level Transient Spectroscopy (Q-DLTS) was performed using same ASMEC assembly. Device structures were also subjected to annealing using rapid thermal processor (GSL-1500X-50RTP). All the fabrication and characterization were done in the Centre for Advanced Electronics and Photovoltaic Engineering (CAEPE).

5.2.3 Characterization of InGaAsP based matrix

Direct band gap-based compound semiconductors are more favorable for photonics due to their prone nature of light matter interactions and tunable band gaps. But the main hindrance that may limits is its growth [92]. In our device design approach, we have adopted n-type InGaAsP deposited over InP substrate and treated under ion- assisted electrical isolation to separate the active layers alongside [93]. This is well established that by ion implantation, surface of host lattice may be damaged due to the inter and intra-atomic collisions [73]. As a result, the physical characteristic of device is likely to alter. After the physical ion implantation, the carrier transport characteristics were investigated to gauge the extent and thermal stability of isolation achieved in the PIC ready platform. A rigorous amount of characterization i.e., current voltage, Arrhenius analysis, transient of charges, carrier transport, kinetics of dark and photo current and Spectroscopic Ellipsometry analysis; has performed for said device matrix.

After initial electrical diagnostics of both ion-assisted devices i.e., pre- and post-implant structures, they were subjected to rapid thermal annealing cycles at 400°C, 500°C, 600°C, 700°C and 800°C for a fixed dwell time of ~60 seconds, in each case.

5.2.3.1 Electrical transport analysis of InGaAsP based PICs

Sheet resistance measurements of C+ and Ni+ implanted devices are performed using four-point technique, with their pre- and post-annealed values are shown in Figure 5.45.

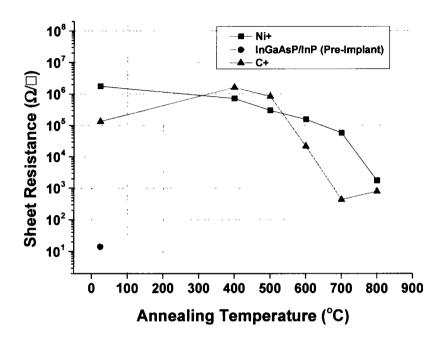


Fig. 5.45: Sheet Resistance of C+ and Ni+ irradiated n-InGaAsP matrix

The doped InGaAsP/InP has very low sheet resistance magnitude when compared with the values obtained after C+ and Ni+ implants i.e. only 13.94 Ω/□. Whereas, the as-implant Ni+ shows one order higher sheet resistance magnitude with respect to C⁺ ion as already depicted in simulation codes (that higher vacancy profile was observed for Ni⁺ case). Also, for Ni⁺ Ion, the extent of damage in form of electrical isolation has 106 times greater with multi-implant energies of 1000 keV and 2000 keV. One may figure out that both implant species behave dynamically with host lattice and one can predict their approximately correct placements within InGaAsP i.e. The Ni⁺ placed themselves very closer to the right lattice sites to form chemical bonding at relatively higher thermal budget and counter the carrier removal which may enhance both, its lattice recovery plus new carrier. Thus, by increasing the annealing temperature, the lattice recovery may provoke injection to the transport cycle of the device operation and

reversal in carrier isolation be observed. For C⁺, there is possibility available to enhance the carrier removal at rather lower annealing temperatures. This is evident for relatively lower temperatures i.e. ~400-500°C. After this temperature window the lattice recovery may increase and contribution in conductivity may be observed readily i.e. at rather higher annealing temperature (~800°C) the magnitude of sheet resistance decreases and ready to approach parent n-InGaAsP characteristics. At this point, the device acts as a carrier transmitter rather than a blocker on operational level.

Another parameter to visualize the carrier dynamics is carrier mobility. For optimum carrier isolation formed in the InGaAsP matrix, the influence of external bias should have either "no" or "lesser" impact when subjected with drift mechanism affecting the carrier's motion into the active/passive regions of the device. Figure 5.46 shows the mobility of both the cases at same annealing temperatures. The initial n-InGaAsP has very high mobility magnitude i.e. 2288.7 cm² /Vs. When C+ and Ni+ ions were bombarded to n-InGaAsP/InP, the carrier mobility decreases up to some certain recessive magnitudes i.e. just resulted into the values of 53 and 196cm²/Vs, respectively. C+ implant when compared with Ni+ implantation, the carrier mobility increases linearly at relatively lower temperatures i.e. ~400-500°C and increases exponentially up to four order of magnitudes at temperatures greater than 500°C. Whereas the Ni+ shows lesser mobility values when we increase annealing temperature beyond 400°C and results in very low magnitudes i.e. ~55cm²/Vs at 800°C.

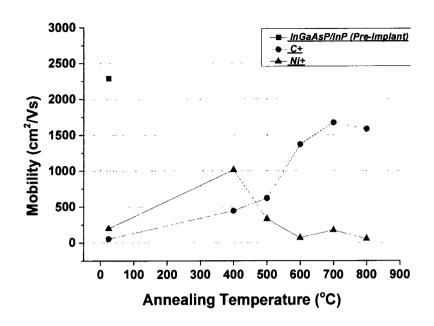


Fig. 5.46: Mobility of C⁺ and Ni⁺ irradiated n-InGaAsP matrix

For effective carrier isolation there should be higher sheet resistances and lower mobilities within active device regions. When one collectively compares both governing parameters i.e. sheet resistance and mobility, a trade-off between both may be considered, while choosing the appropriate annealing temperature for device processing. For C^+ , $400\text{-}500^\circ\text{C}$ annealing temperature have sufficient magnitudes of sheet resistances ($\sim 10^6\Omega/\square$) and lower mobility ($\sim 450\text{-}600\text{cm}^2/\text{Vs}$) for the device isolation. For Ni⁺, only the 500°C processed devices show the sufficient values of sheet resistances ($\sim 105\Omega/\square$) and lower mobility magnitudes (~ 331 cm²/Vs). Thus, for both the implant cases 500°C of annealing cycle with 60s dwell may provide sufficient carrier isolation from n-InGaAsP device matrix. The behavior of isolation due to the used implant strategy, it is evident that C^+ shows higher carrier removal phenomena compared with Ni⁺. Further, C^+ ion-assisted electrical isolation in the n⁺-InGaAsP/InP may well be due to the ion induced damage accumulation in the region whereas Ni⁺-implants tend to reflect chemical isolation phenomenon.

5.2.3.2 Current-Voltage analysis of InGaAsP based PICs

To evaluate carrier isolation approach in a more practical manner, one may investigate the carrier dynamics by varying the drift force in terms of external electric field and record the directional motion of carriers and their effective magnitudes. For this, we have performed twopoint Current-Voltage (I-V) measurements to evaluate the drift driven carrier's popping. Figure 5.47 shows the I-V analysis of all pre- and post-implant. For effective carrier isolation there should be higher sheet resistances and lower mobilities within active device regions. When one collectively compares both governing parameters i.e. sheet resistance and mobility, a trade-off between both may be considered, while choosing the appropriate annealing temperature for device processing. For C⁺, 400-500°C annealing temperature have sufficient magnitudes of sheet resistances ($\sim 10^6 \Omega/\Box$) and lower mobility ($\sim 450-600 \text{cm}^2/\text{Vs}$) for the device isolation. For Ni⁺, only the 500°C processed devices show the sufficient values of sheet resistances ($\sim 10^5 \Omega/\Box$) and lower mobility magnitudes (~331 cm²/Vs). Thus, for both the implant cases 500°C of annealing cycle with 60s dwell may provide sufficient carrier isolation from n-InGaAsP device matrix. The behavior of isolation due to the used implant strategy, it is evident that C⁺ shows higher carrier removal phenomena compared with Ni⁺. Further, C⁺ ion-assisted electrical isolation in the n⁺-InGaAsP/InP may well be due to the ion induced damage accumulation in the region whereas Ni⁺-implants tend to reflect chemical isolation phenomenon.

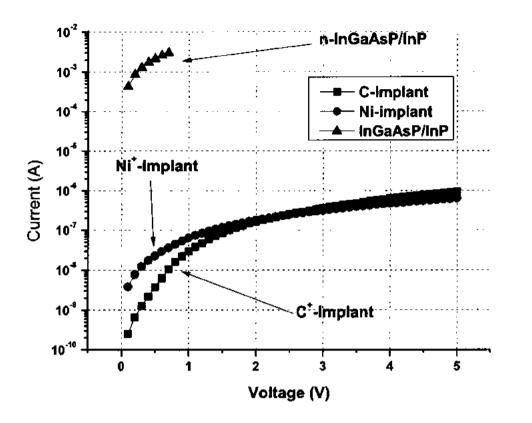


Fig. 5.47: Current-Voltage analysis of C+ and Ni+ irradiated n-InGaAsP matrix

From SRIM we predicted that the transmitted ions through n-lnGaAsP layer for C⁺ and Ni⁺ are ~90 and 38%, respectively. Thus, 10% for C⁺ and 62% for Ni⁺ ions have become a part of n-lnGaAsP lattice and rest of ions are departed and placed themselves into n-lnGaAsP/lnP interface and bulk. The majority of C⁺ ions have placed themselves into the top layer of lnP substrate. The internal chemistry between subjected ions and In, Ga, As and P atoms have to decide the electromigration under subject drift electric fields. Figure 6 shows the carrier migration (current flow) for base (n-lnGaAsP) and as- ion implanted device matrix. The electric field is directly dependent that may provide a pushup force to electro-migrate the free carriers from their fermi-level edges. For electric filed (<1.5V), the carrier's removal/isolation capacity of C⁺ is dominant and provides less free carriers that may jump into the conduction (10⁻¹⁰-10⁻⁹A). For rather higher electric fields, this behavior is more evident. After 1.5V, for both as-implant cases, the influence of electric field acts same and contribute almost same

number of carriers that may be captured by drift mechanism and become free to move into the lattice.

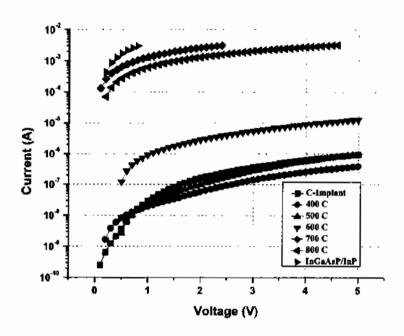


Fig. 5.48 (a): Current-Voltage analysis of C* ion annealed at multiple temperatures

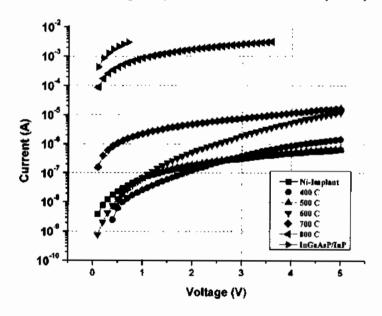


Fig. 5.48 (b): Current-Voltage analysis of post Ni⁺ implanted and annealed devices at multiple temperatures. Likewise, the impact of drift electric field for both C⁺ and Ni⁺ implant cases of variable annealing temperatures is shown in Figures 5. 48(a-b).

Figure 5.48 shows that by increasing the annealing temperature, the availability of carriers for device operation increases. There are two possibilities available behind their incremented magnitudes i.e. one is the parent lattice recovery (ion induced damage recovery resulting into transmittances) and the other is percentage of C⁺ and Ni⁺ ions that are present within the n-InGaAsP lattice and may bond with InGaAsP atoms (residue doping). The path of charge leakage at the InGaAsP/InP interface where majority of the ions are localized, contributes excess of drift currents to the system. This can be visualized that electric field directly impacts and may enhance the electro-migration of free carriers i.e. same devices annealed at multiple temperatures would act differently when subjected to low or relatively higher fields. This is true for both the implant strategies, for example, current magnitudes are greater (when compared with 500°C) and becomes significantly lowers for relatively higher electrical fields (>0.7V). Similar behavior is evident from Ni⁺ case too and for C⁺ implanted and annealed at 400°C case.

5.2.3.3 Arrhenius analysis (I-V) of InGaAsP based PICs

One of another parameters is Activation Energy that has readily been treated as diagnostic parameter to evaluate the extent of minimum energy needed for the conduction of already available (but in minute amount) carrier within the ion assisted damaged region [73]. For better isolation the amount of this energy should be high enough so that only few carriers may coupe up under certain drift mechanism. The formulism [73] that governs the activation energy is given in Equation 5.11 (commonly known as Arrhenius Equation) below:

$$\sigma_{S} = \sigma_{0} e^{\frac{E_{A}}{KT}}$$
 (5.11)

Where ' σ_S ' is the conductivity at a given temperature, ' σ_o ' is the conductivity at absolute temperature, 'K' is the Boltzmann's constant (=8.617×10⁻⁵ eVK⁻¹), 'T' is temperature in

kelvin and 'E_A' is the activation energy. By linearizing of Equation 5.41 one can obtained the value of activation energy. The linearized equation is given as 5.12:

$$ln \sigma_S = (EA/1000K)(1000/T) + ln \sigma_0$$
 (5.12)

In our design, we scanned I-V analysis (which gives the values for conductivity) in both the ion implanted cases, which are annealed over temperature ranges from 300K to 340K (in-situ) in order to gauge the activation energies of the process.

5.2.3.3.1 Arrhenius analysis (I-V) of InGaAsP (bare, Ni⁺ Implanted and Annealed)

For Arrhenius analysis I-V measurements have been recorded at temperatures 300K, 310K, 320K, 330K and 340 K and presented in Figures 5.49, 5.50, 5.51, 5.52, 5.53, 5.54 and 5.50 below:

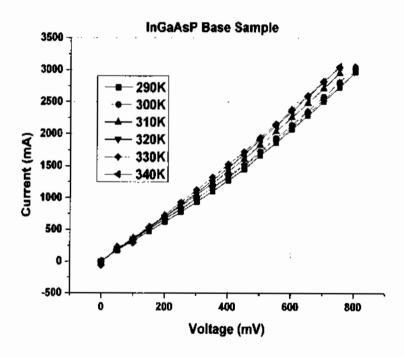


Fig. 5.49: Arrhenius analysis of InGaAsP (as grown sample)

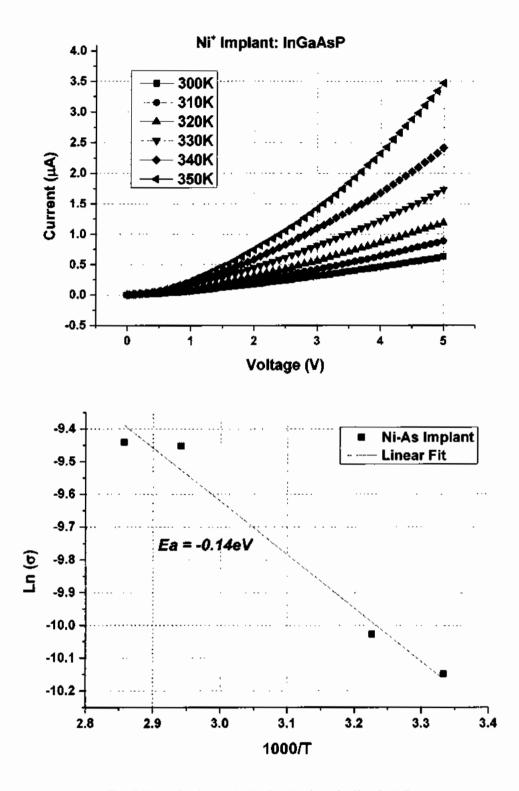


Fig. 5.50: Arrhenius analysis of as Implanted Ni* InGaAsP

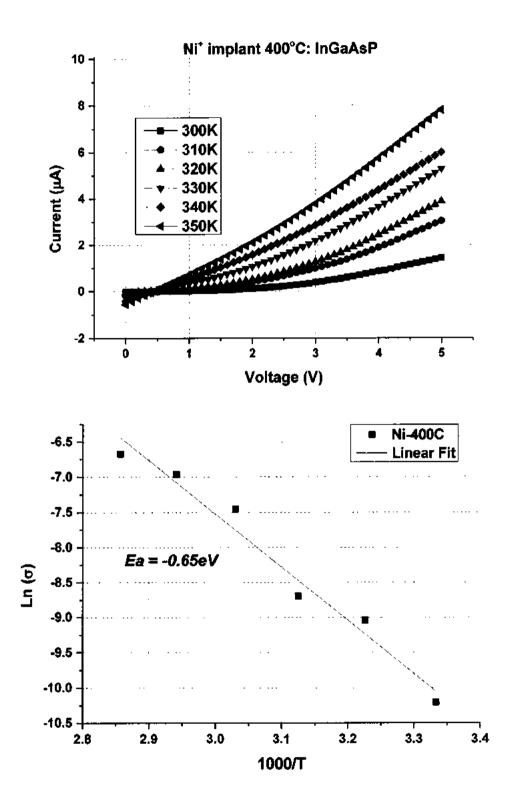
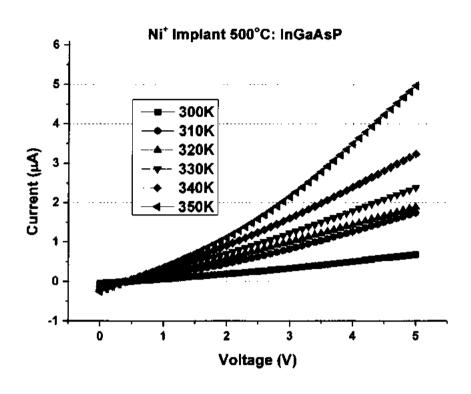


Fig. 5.51 Arrhenius analysis of Ni⁺ Implanted InGaAsP Annealed at 400°C



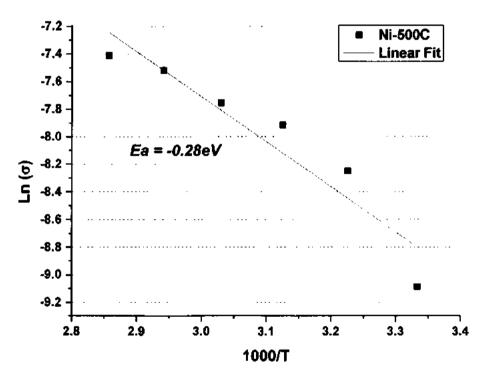
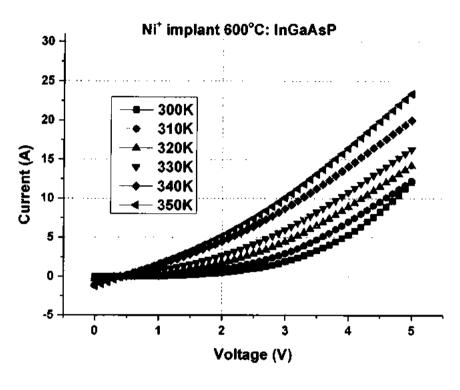


Fig. 5.52: Arrhenius analysis of Ni⁺ Implanted InGaAsP Annealed at 500°C



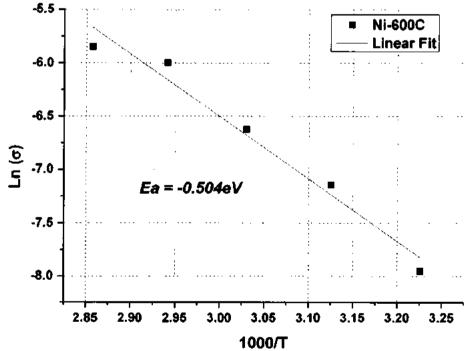


Fig.5.53: Arrhenius analysis of Ni⁺ Implanted InGaAsP Annealed at 600°C

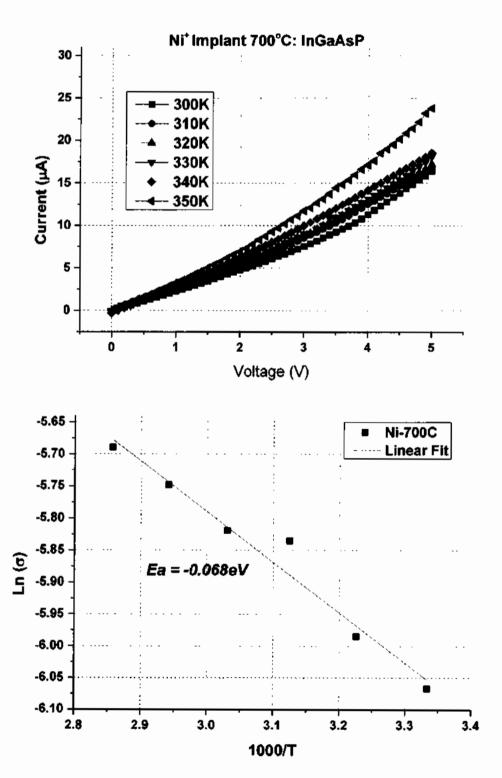


Fig. 5.54: Arrhenius analysis of Ni¹ Implanted InGaAsP Annealed at 700°C

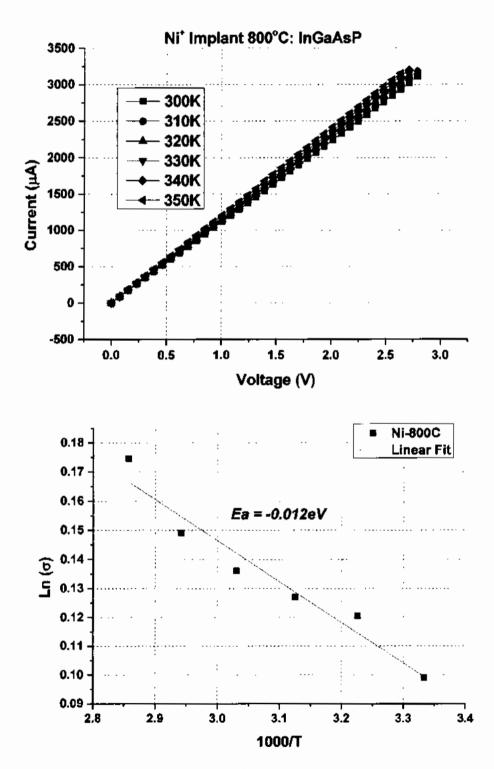


Fig. 5.55: Arrhenius analysis of Ni⁺ Implanted InGaAsP Annealed at 800°C

5.2.3.3.2 Arrhenius analysis (I-V) of InGaAsP (C+ Implanted and Annealed)

For Arrhenius analysis I-V measurements have been recorded at temperatures 300K, 310K, 320K, 330K and 340 K and presented in Figures 5.56, 5.57, 5.58, 5.59, 5.60 and 5.61 below:

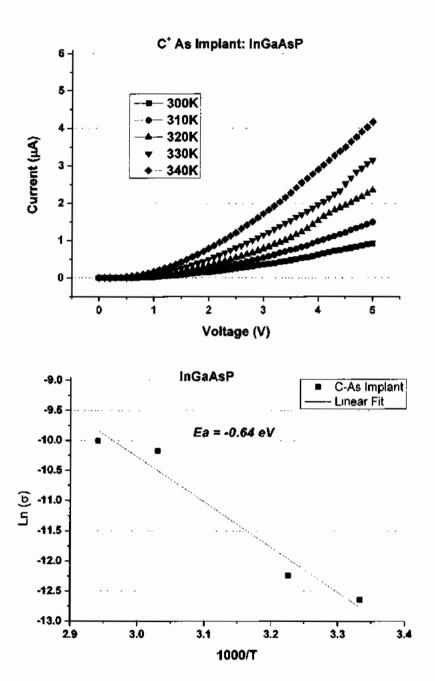


Fig.5.56: Arrhenius analysis of as Implanted C+ InGaAsP

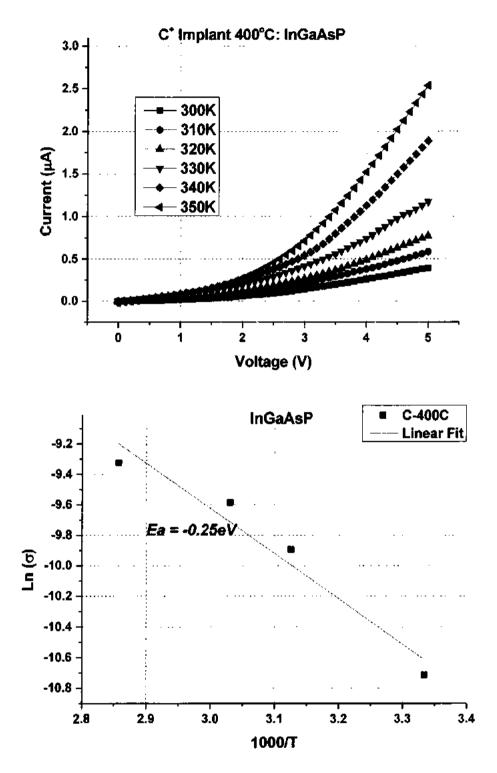
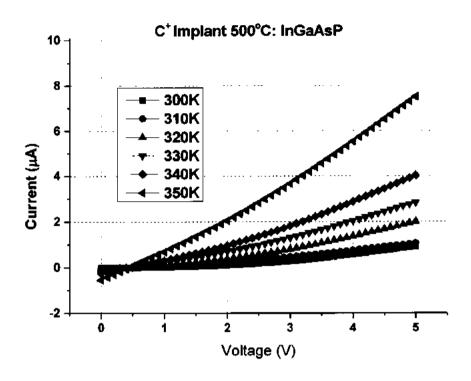


Fig. 5.57: Arrhenius analysis of C⁺ Implanted InGaAsP Annealed at 400°C



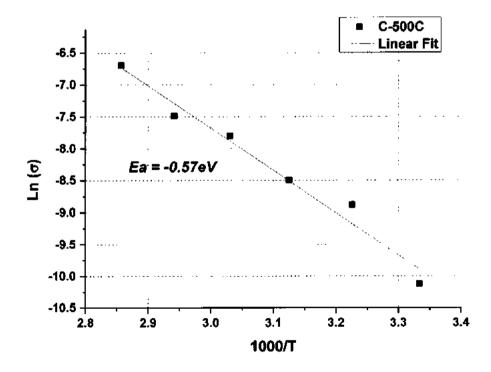
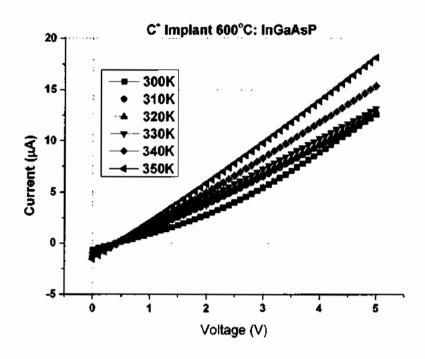


Fig.5.58 Arrhenius analysis of C⁺ Implanted InGaAsP Annealed at 500°C



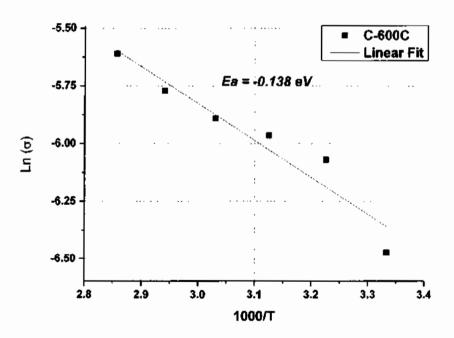
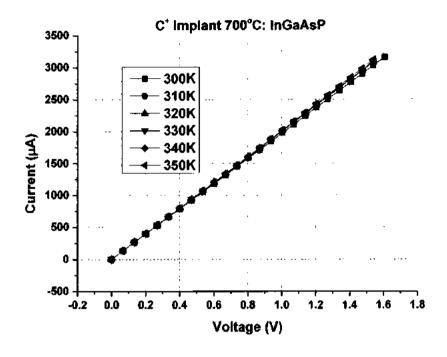


Fig.5.59 Arrhenius analysis of C+ Implanted InGaAsP Annealed at 600°C



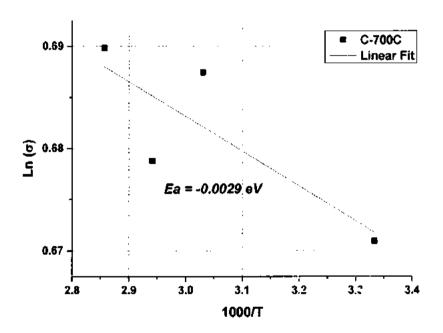
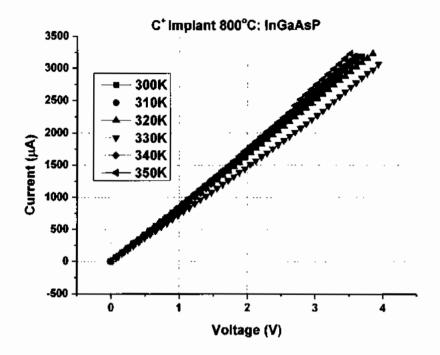


Fig. 5.60: Arrhenius analysis of C⁺ Implanted InGaAsP Annealed at 700°C



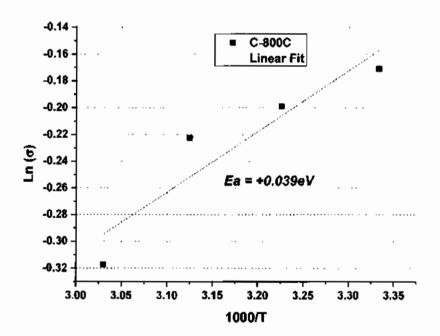


Fig. 5.61 Arrhenius analysis of C* Implanted InGaAsP Annealed at 800°C

5.2.3.3.3 Summary: Current-Voltage based Arrhenius Analysis

Case-wise activation energies (E_A) calculated from Equation 5.12 are collectively shown in Figure 5.62. Activation energies provide a direct assessment about the energies needed for the proper conduction of carriers present within the implanted region of InGaAsP device. Thus, parent n-InGaAsP device would provide very low activation energies because conduction of charges can take place owing the available carriers present in the field. In our carrier isolation approach, we need large amount of energy to conduct. Thus, large activation energies are desirable for ion induced damage placed regions.

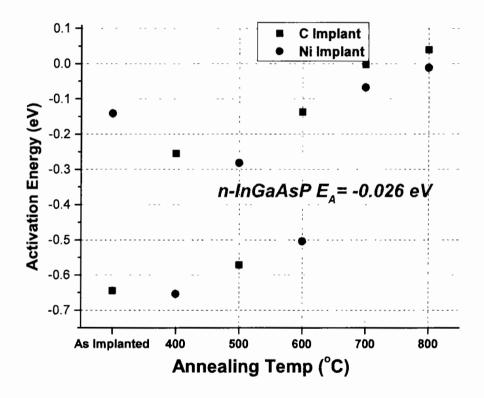


Fig. 5.62: Activation Energies of C+ and Ni+ implanted InGaAsP matrix

Figure 5.62 shows activation energy magnitudes for all discussed devices. Negative sign shows that the temperature coefficient of resistance (TCR) is negative for all said cases i.e., by increasing the temperature, resistance of the sample decreases and can be visualized further from Figure 5.48. The activation energy (E_A) of parent n-InGaAsP is very low i.e., -0.026eV. Which means very low amount of energy needed for the conduction and can be observed from

Figure 5.48. When this matrix has subjected with C⁺ and Ni⁺, large amount of disorder has prevailed and the sense of electro-migration in that specific region has calculated using Equation 5.12. This has shown that for C⁺ implant case, as-implant scheme needs much energy to surmount the energy barrier. Thus, better isolation may conceive in form of energy scales i.e., -0.64eV energy would need for minimum conduction. For Ni⁺, just -1.5eV energy has recorded for same case. This magnitude decreases by increasing the annealing temperature. By keeping these aforementioned parameters into account i.e. Sheet Resistance, Mobility, Current-Voltage profiles; it seems that there would be a trade-off between all said cases. For all, C⁺ at 500°C annealing temperature provides good trade-off when dealt with all said parameters.

5.2.3.4 Kinetics of Dark and Photo Current

To inspect the photon driven carrier activation in GaN-based PIC platform, kinetics of electric current under dark and luminous condition at variable electric field was also performed. We have specially employed these measurements at zero applied bias, as well, to inspect the photo-induced charge voltaicity phenomena, for both the implant cases (Ni⁺ and C⁺ Implant).

5.2.3.4.1 Kinetics of Photo Current of C⁺ Implanted n-InGaAsP based PIC Platform (As Implanted and Annealed)

In this section, the case wise manipulation of C⁺ implanted n-InGaAsP based Matrix for PICs has been discussed in detail. We have made all the measurements under different biased conditions i.e., from 0V (absence of bias) to 5V. All these measurements have been presented below in Figs. 5.63, 5.64, 5.65, 5.66, 5.67 and 5.68. These graphs provide an overview of the variation in dark and photo currents as C⁺ implanted sample have been annealed and subsequently measurements were carried out under different biasing conditions.

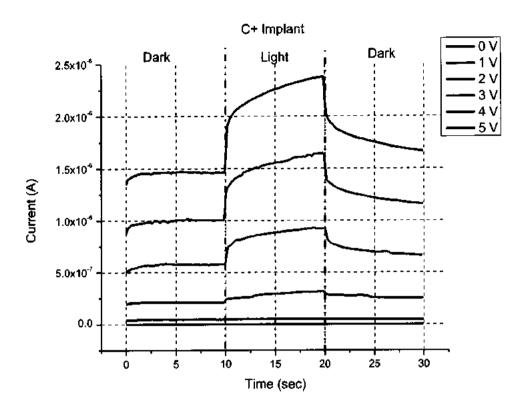


Fig. 5.63: Kinetics of Dark and Photo current for as C+ Implanted case

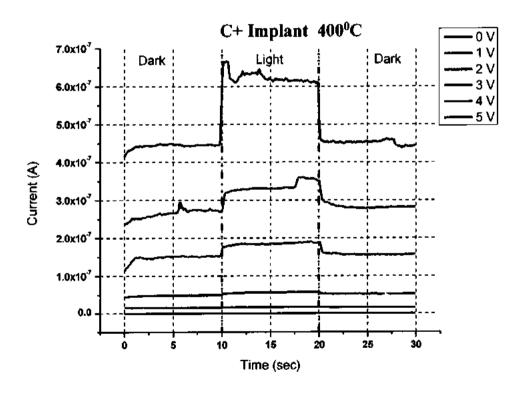


Fig. 5.64: Kinetics of Dark and Photo current for C+ Implanted annealed at 400°C

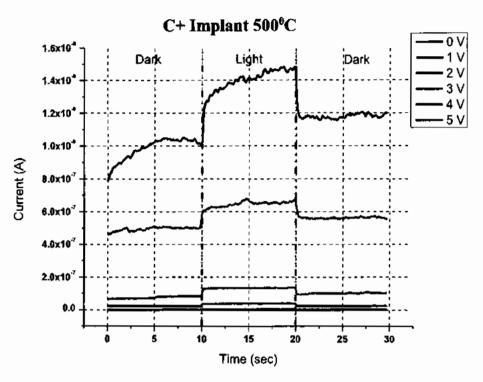


Fig. 5.65 Kinetics

of Dark and Photo current for C+ Implanted annealed at 500°C

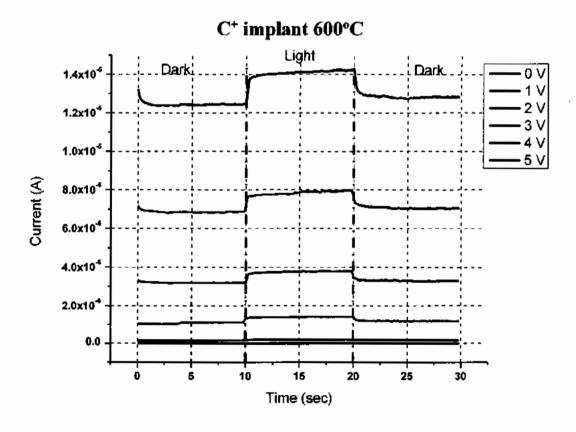


Fig. 5.66: Kinetics of Dark and Photo current for C+ Implanted annealed at 600°C

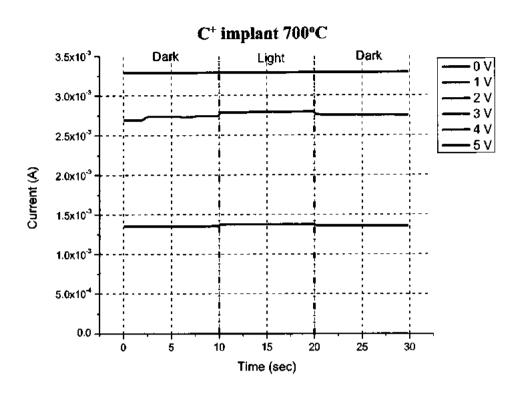


Fig. 5.67: Kinetics of Dark and Photo current for C+ Implanted annealed at 700°C

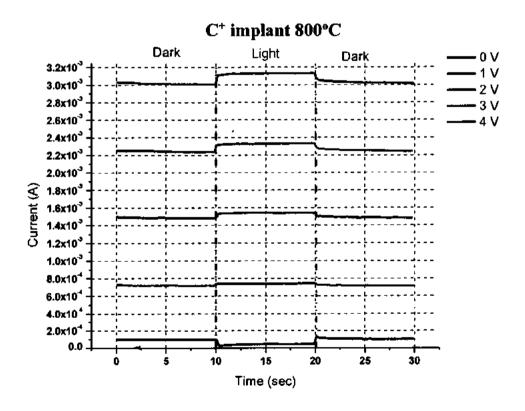


Fig.5.68: Kinetics of Dark and Photo current for C+ Implanted annealed at 800°C

5.2.3.4.2 Effect of Annealing on Kinetics of Dark and Photo Current for C+ Implant

Here keeping the drift constant, the effect of annealing on the kinetics of dark and photo current have been elaborated. For this purpose, we have selected two biases i.e., 0V (absence of drift) and 5V (maximum drift). These effects have been clearly elaborated in Figs.5.69 and 5.70 below.

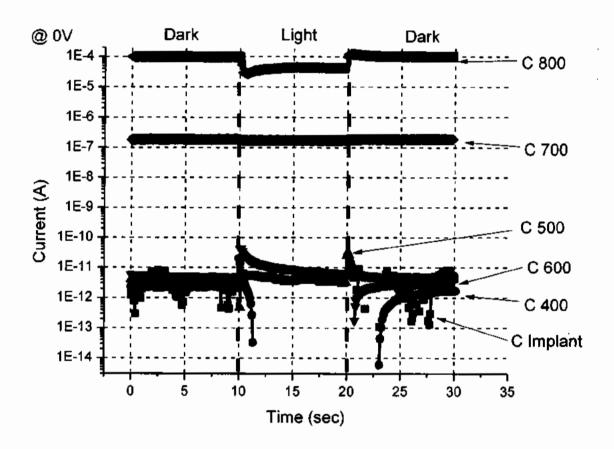


Fig. 5.69 Kinetics of Dark and Photo current for C* implanted InGaAsP at 0V

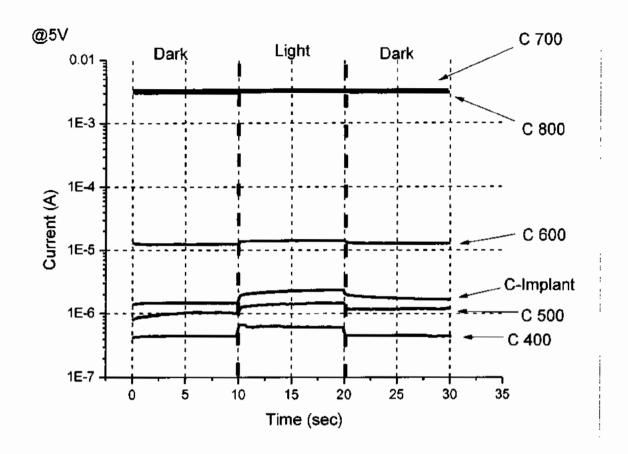


Fig. 5.70: Kinetics of Dark and Photo current for C+ implanted InGaAsP at 5V

5.2.3.4.3 Kinetics of Photo Current of Ni⁺ Implanted n-InGaAsP based PIC Platform (As Implanted and Annealed)

In this section, the case wise manipulation of Ni⁺ implanted n-InGaAsP based Matrix for PICs has been discussed in detail. We have made all the measurements under different biased conditions i.e., from 0V (absence of bias) to 5V. All these measurements have been presented below in Figs. 5.71, 5.72, 5.73, 5.74, 5.75 and 5.76. These graphs provide an overview of the variation in dark and photo currents as Ni⁺ implanted sample have been annealed and subsequently measurements were carried out under different biasing conditions.

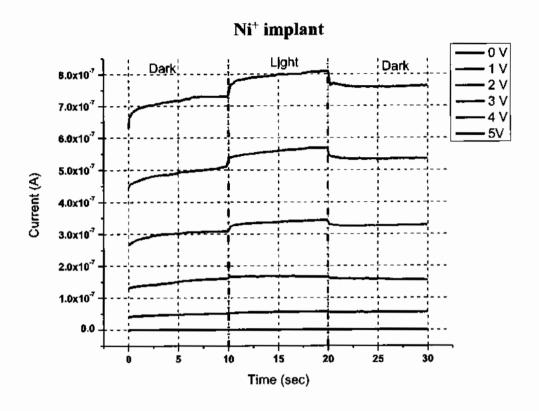


Fig. 5.71: Kinetics of Dark and Photo current for as Ni⁺ Implanted case

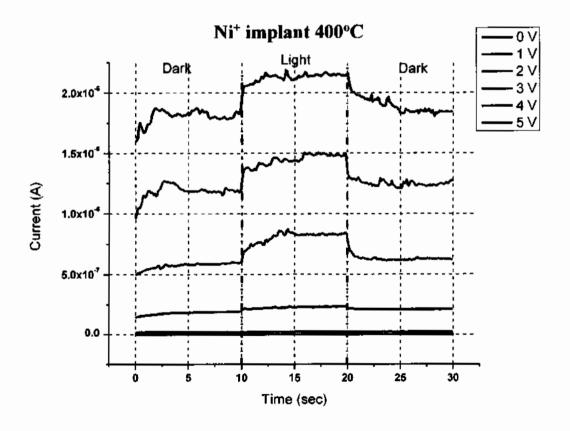


Fig. 5.72: Kinetics of Dark and Photo current for Ni⁺ Implanted annealed at 400°C

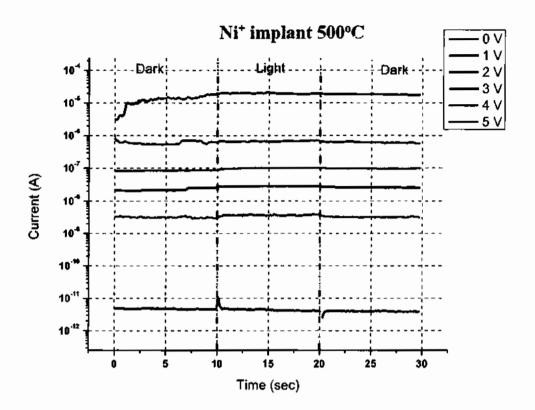


Fig. 5.73: Kinetics of Dark and Photo current for Ni⁺ Implanted annealed at 500°C

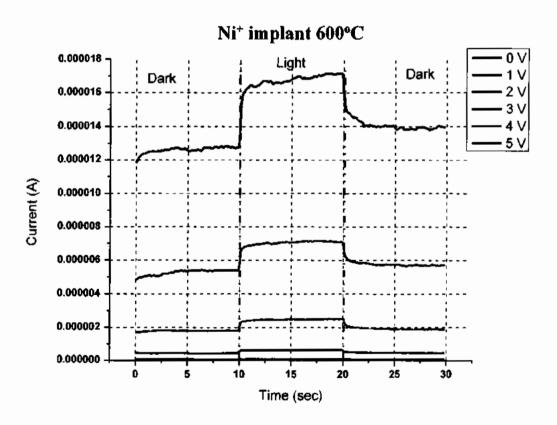


Fig. 5.74: Kinetics of Dark and Photo current for Ni* Implanted annealed at 600°C

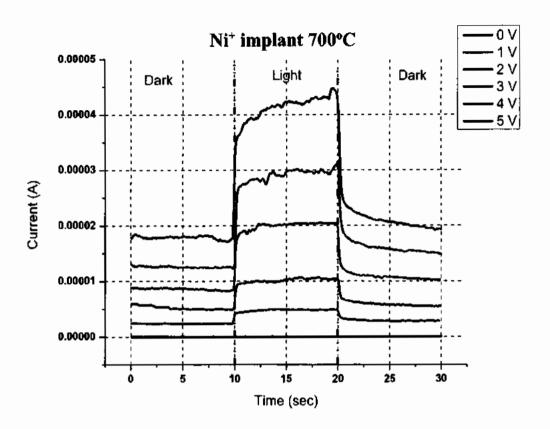


Fig. 5.75: Kinetics of Dark and Photo current for Ni⁺ Implanted annealed at 700°C

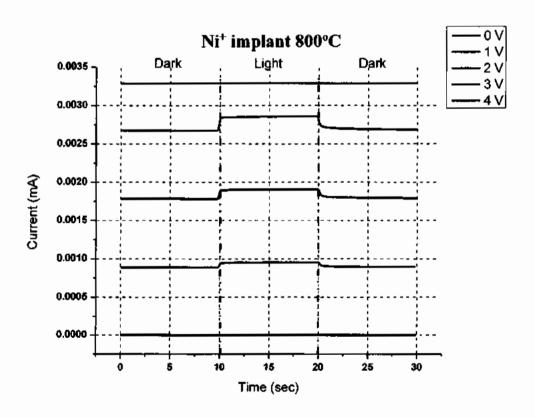


Fig. 5.76: Kinetics of Dark and Photo current for Ni⁺ Implanted annealed at 800°C

5.2.3.4.4 Effect of Annealing on Kinetics of Dark and Photo Current for Ni⁺ Implant

Here keeping the drift constant, the effect of annealing on the kinetics of dark and photo current have been elaborated. For this purpose, we have selected two biases i.e., 0V (absence of drift) and 5V (maximum drift). These effects have been clearly elaborated in Figs.5.77 and 5.78 below.

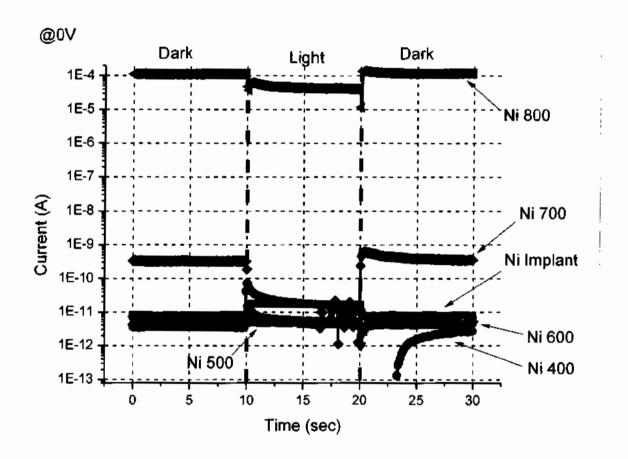


Fig. 5.77: Kinetics of Dark and Photo current for Ni⁺ implanted InGaAsP at 0V

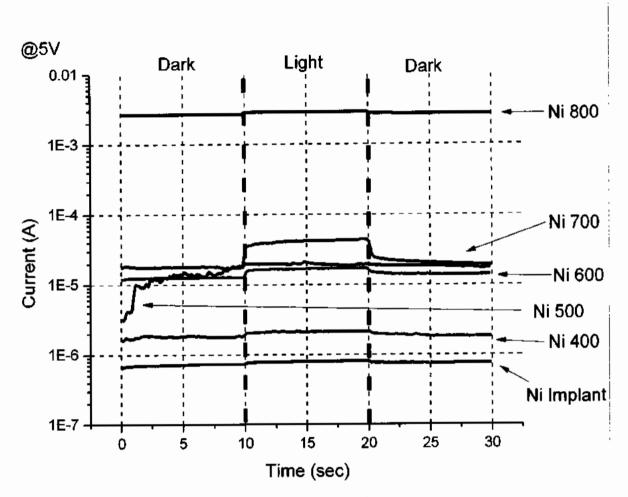


Fig. 5.78: Kinetics of Dark and Photo current for Ni⁺ implanted inGaAsP at 5V

The exact values of dark and luminous currents under different bias conditions achieved after repetitive measurements are reported in Table 5.7 and 5.8 for, C⁺ and Ni⁺ ions respectively. These are the magnitudes of dark and photo currents under multiple biased conditions that we have already pointed for 0V and 5V bias regimes under fixed optical power. From these two tables one may clearly see that how much current have been increased by incident photons at a particular implanted region.

Table 5.7: Dark and photo current under different bias conditions for C Ion Implant

Sample	@(V		&iA		@ZV		@ 3∀		@ 4∀		@SV	
	Dark	Light	Dark	Light	Dark	Light	Derk	Light	Dark	Light	Dark	Light
C'-imp	4.97×10	3.59×10 ⁻	4.48×10	5.11×10	2.08×10	3.14x10	571×10	9.27×10 ⁻	1x10 ⁻⁶	1.65x10	1 44×10	2.37x10
C'400	1.16x10 u	2.02x10-	1.59x10 ⁻	1.75×10 *	4.84×10·	5.77x10	1.44×10	1.91×10	2.69×10 ⁻	3.6x10 ^{-/}	4.43x10 ⁻	6.65×10
C+500	1.38x10	3.25x10	2.46x10	3.7x10°	2.3x10*	4.03x10	7.09×10	1.36x10	4.84×10	6.78×10	1×10 °	1.48×10-
C*600	1.01×10	4.33x10 ⁻	1.48x10	2.01x10	1.09×10	1.42×10-	3.17×10	3.8×10 ⁻⁶	6.7×10*	7.97x10	1.24×10	1.42×10 ⁻
C*700	1.82×10 ⁻⁷	1.7x10 ⁻⁷	0.00135	0.00137	0.00272	0.00279					-	
C*800	9.77x10 ⁻ s	2.67x10 ⁻	7.18x10 ⁻	7.44x10	0.00147	0 00154	0.0022	0.0023	0.003	0.0031	-	-

Table 5.8: Dark and photo current under different bias conditions for Ni Ion Implant

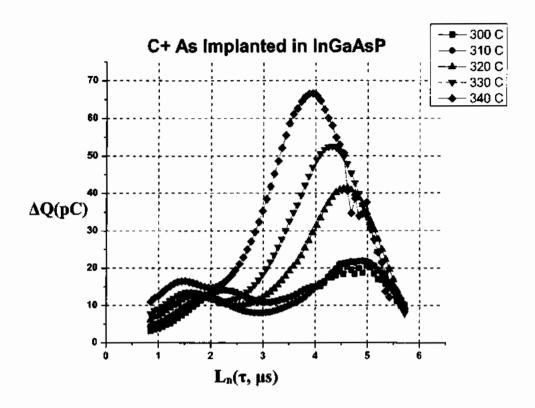
Semple	⊕ 0∨		@ 1V		@2V		@3V		@4 V		@5V	
-	Dark	Light	Dark	Light	Dark	Light	Derk	Light	Dark	Light	Dark	Light
Ni*imp	8.2×10 ⁻	1 79x10 ⁻	4.77x10	5.69x10	1.5x10 ⁻⁷	1.68×10	2.96x10	3.43x10 ⁻⁷	4.83x10 ⁻	5.68x10	7.17x10	8.09x10
Ni*400	3 41×10	7.4x10 ⁻¹¹	2.04x10	2.37x10	1.86x10	2.34x10	5.5×10 ⁻⁷	8 7x10 ⁻⁷	1.15x10	1.5x10*	1.78×10	2.18×10
Ni*500	2.98x10	1 05×10	2.89×10	3.93×10	2.17×10	2.88×10	8.42×10	1.037x10	5.31x10	7.08x10 ⁻	1 29×10	2 1×10 ⁻⁵
NI+600	1 01x10·	1.3x10 ⁻¹¹	5.45×10 ⁻	8x10*	4 09×10	5.34×10 ⁻	1.78x10-	2.52x10*	5.06x10 ⁻	7 16x10 ⁻	1.25x10 ⁻	1.71×10
Ni*700	6.2x10	2.97x10 ⁻	2.34x10 ⁻	4.98x10	4 89×10·	1.07x10 ⁻	8 24×10	2.05x10 ⁻⁵	1 22×10	3.13x10 ⁻	1 7×10-5	4.46x10 5
Ni*800	1.4x10 ⁻	6.2x10 ⁻¹¹	8 8x10 ⁻⁴	9.5x104	0.00178	0.0019	0.00267	0.002859	-	-		

5.2.3.5 Charge transient (Q-DLTS) analysis of InGaAsP based PICs

A detailed analysis of Charge transients has performed in order to observe the migration of induced trapped charges by the drift pump mechanism providing an insight to the electronic defects or trapping centers. The influence of light and field on these centers will be of importance on device level when intra-device isolation is desirable to achieve on PIC's substrate. A Charge based Deep Level Transient Spectroscopy (Q-DLTS) has been performed on both the implant cases, in order to study the impact of trap levels placed within the energy band picture and its associated characteristics that may be generated by the migration process of alien ion species.

5.2.3.5.1 Charge Transient Analysis for C⁺ Implanted InGaAsP based PIC Platform (As Implanted and Annealed)

In order to investigate the trap parameters i.e. trap densities (N_T), Capture cross section (σ), and trap level energy (E_T); The charge transient analysis of C⁺ implanted n-InGaAsP matrix has been characterized. For all annealed C⁺ implanted samples; the samples were measured at 300K, 310K, 320K, 330K, 340K and 350K ambient temperatures and by linear approximation of Equation 5.8 (also called Arrhenius analysis), the trap energy (Ea) and capture cross section have been calculated. For trap concentration Equation 5.10 has been used. These analyses have been presented in Figs. 5.79, 5.80, 5.81 and 5.82 below:



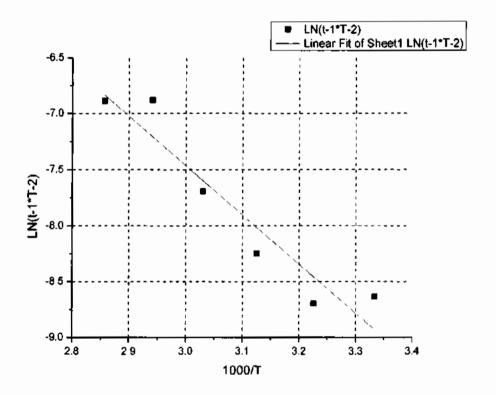
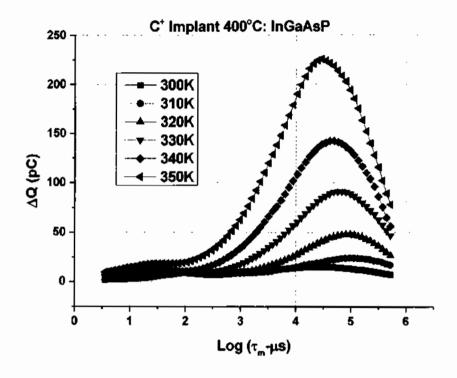


Fig. 5.79: Arrhenius Analysis of as Implant C+ ion



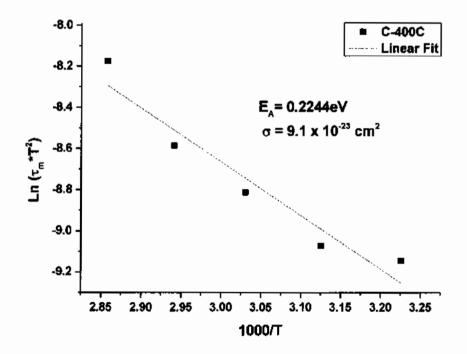
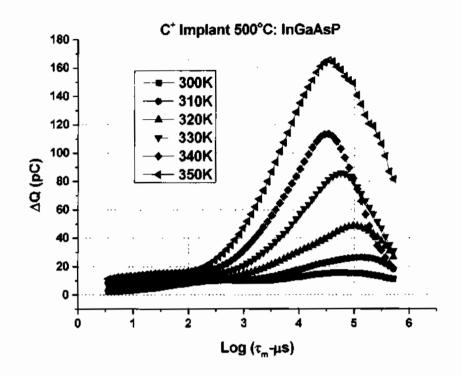


Fig. 5.80: Arrhenius Analysis of C⁺ implant annealed at 400°C



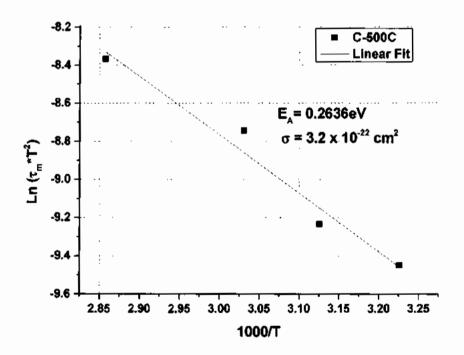


Fig. 5.81: Arrhenius Analysis of C+ implant annealed at 500°C

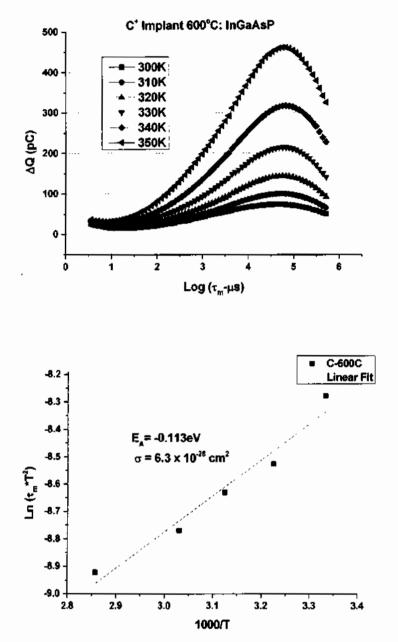
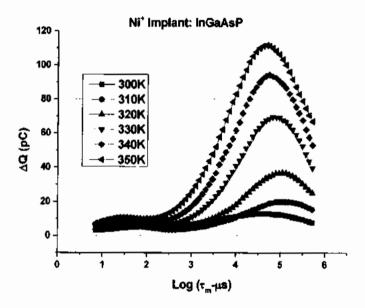


Fig. 5.82: Arrhenius Analysis of C+ implant annealed at 600°C

5.2.3.5.2 Charge Transient Analysis for Ni⁺ Implanted InGaAsP based PIC Platform (As Implanted and Annealed)

In order to investigate the trap parameters i.e. trap densities (N_T), Capture cross section (σ), and trap level energy (E_T); The charge transient analysis of Ni⁺ implanted n-InGaAsP matrix has been characterized. For all annealed Ni⁺ implanted samples; the samples were measured at

300K, 310K, 320K, 330K, 340K and 350K ambient temperatures and by linear approximation of Equation 5.8 (also called Arrhenius analysis), the trap energy (Ea) and capture cross section have been calculated. For trap concentration Equation 5.10 has been used. These analyses have been presented in Figs. 5.83, 5.84, 5.85, 5.86 and 5.87 below:



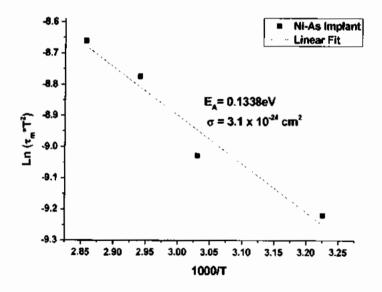
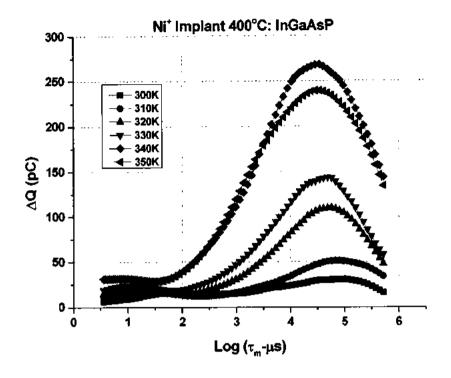


Fig. 5.83: Arrhenius Analysis of as Implant Ni* ion



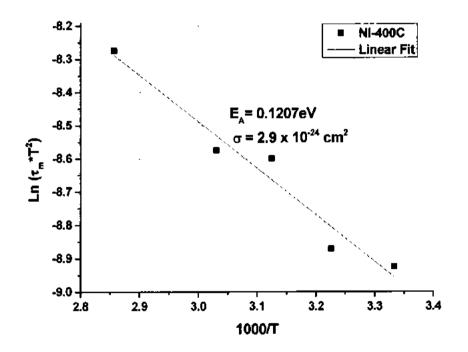
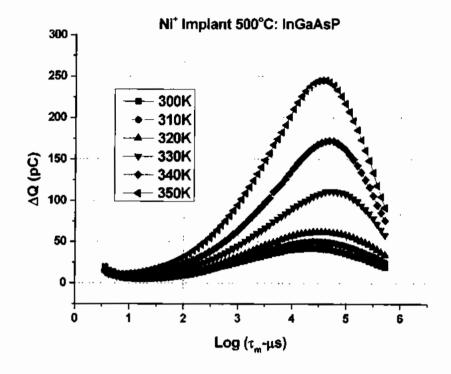


Fig. 5.84: Arrhenius Analysis of Ni⁺ implant annealed at 400°C



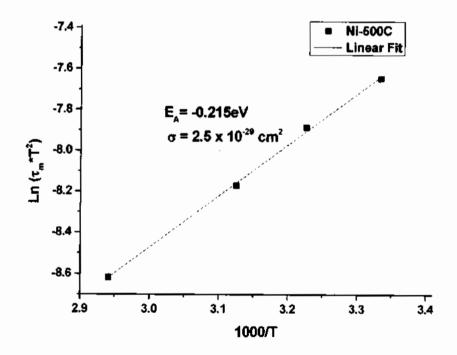
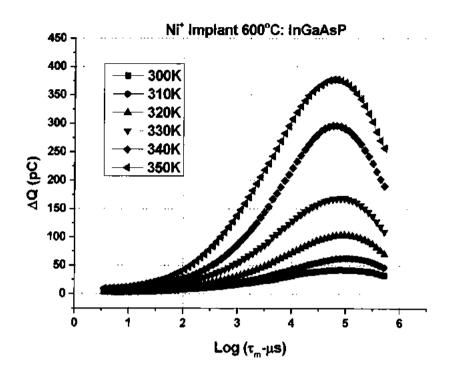


Fig. 5.85: Arrhenius Analysis of Ni⁺ implant annealed at 500°C



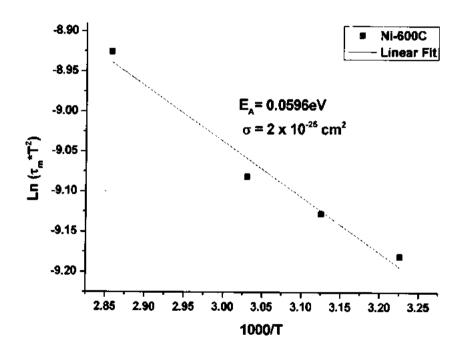
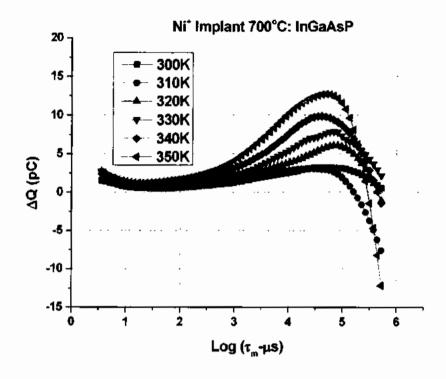


Fig. 5.86: Arrhenius Analysis of Ni⁺ implant annealed at 600°C



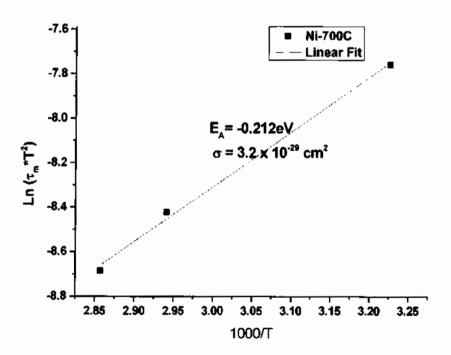


Fig. 5.87: Arrhenius Analysis of Ni⁺ implant annealed at 700°C

All the above results have been summarized in the Table 5.9 below:

Table 5.9: Trap parameters of C⁺ and Ni⁺ for InGaAsP active device matrix

Anneal . Temp	Imp lant Ion	N _T (cm ⁻²)						E _A (eV)	σ (cm²)
		@ 300K	@ 310K	@ 320K	@ 330K	@ 340K	@ 350K	(64)	(cm)
As- Implant	C^+	2.11x10 ¹¹	2.34x10 ¹¹	4.40x10 ¹¹	5.59x10 ¹¹	7.09x10 ¹¹		0.3786	6.4x10 ⁻²⁰
	Ni ⁺	1.39x10 ¹¹	2.12x10 ¹¹	3.90x10 ¹¹	7.38x10 ¹¹	9.97x10 ¹¹	1.18x10 ¹²	0.1338	3.1x10 ⁻²⁴
400 °C	C^+	1.57x10 ¹¹	2.54x10 ¹¹	5.08x10 ¹¹	9.69x10 ¹¹	1.51x10 ¹²	2.39x10 ¹²	0.2244	9.1x10 ⁻²³
	Ni ⁺	3.28x10 ¹¹	5.44x10 ¹¹	1.17x10 ¹²	1.53x10 ¹²	2.85x10 ¹²	2.54x10 ¹²	0.1207	2.9x10 ⁻²⁴
500 °C	C^{+}	1.64x10 ¹¹	2.81x10 ¹¹	5.15x10 ¹¹	9.11x10 ¹¹	1.21x10 ¹²	1.75x10 ¹²	0.2636	3.2x10 ⁻²²
	Ni ⁺	4.48x10 ¹¹	5.36x10 ¹¹	6.60x10 ¹¹	1.18x10 ¹²	1.83x10 ¹²	2.6x10 ¹²	-0.215	2.5x10 ⁻²⁹
600 °C	C^+	7.85x10 ¹¹	1.07x10 ¹²	1.52x10 ¹²	2.27x10 ¹²	3.37x10 ¹²	4.89x10 ¹²	-0.113	6.3x10 ⁻²⁸
	Ni ⁺	4.47x10 ¹¹	6.64x10 ¹¹	1.10x10 ¹²	1.79x10 ¹²	3.15x10 ¹²	4.01x10 ¹²	0.0596	2.0x10 ⁻²⁵
700 °C	Ni ⁺	3.44x10 ¹⁰	3.26x10 ¹⁰	6.46x10 ¹⁰	8.37x10 ¹⁰	1.04x10 ¹¹	1.35x10 ¹¹	-0.212	3.2x10 ⁻²⁹

This has noticed that as the temperature increases the trap concentration also increases, however, for Ni⁺ annealed at 400°C that the trap density at 350K is slightly lesser then 340K, it may because of the lesser discharge transient are recorded for 350K when compared with 340K one. As in Q-DLTS the spectra is dividend of charge transients as mentioned in Figure 5.18, thus, there is a possibility available at any temperature to reduce the change in charge magnitude this may because of RC time constant of subject lattice when biased externally (also mentioned in Figure 5.18).

5.2.3.5.3 Comparison of Ni⁺ and C⁺ Implants based on Charge Transient Analysis

As per Equation 5.10, higher the ΔQ magnitude higher will be the trap densities/concentration i.e. $N_T \alpha \Delta Q_{max}$. From initial assessment (i.e. as-implant cases) as shown in Figure 5.88, the higher trap densities are present in C^+ case when relatively compared with its Ni^+ counterpart. This phenomenon may readily be understood by the transmitted ions not from the lattice voids (vacancies profiles) because if the ions are part of the InGaAsP's lattice there is a higher

probability to contribute during the conduction process. Thus, the impact of charged trap region in form of voids and interstitials due to ion-induced damage and provides an equivalent parasitic RC coupling on circuit level.

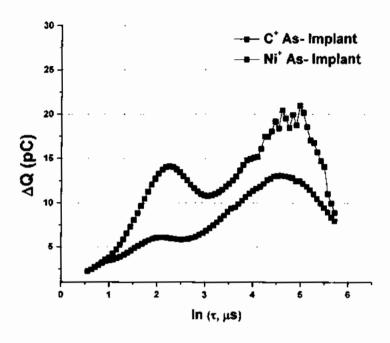


Fig. 5.88: Q-DLTS analysis of as-implant cases

The case-wise transients of as-implant and annealed of Ni+ and C+ devices are shown in Figure 89, separately. The surface trap concentrations of each such case has been calculated from Equation 5.10 and summarized in Table 5.9.

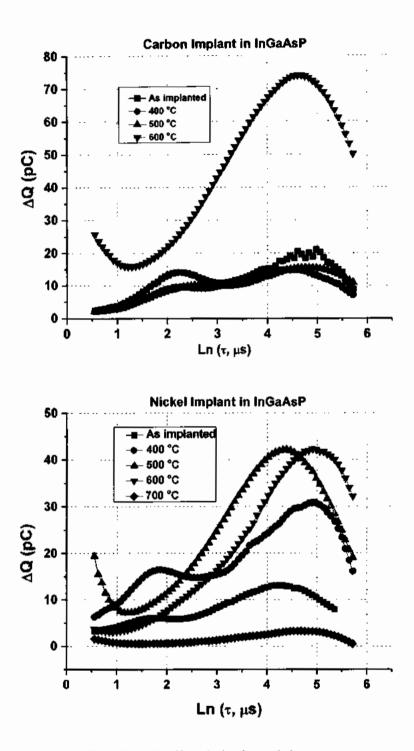


Fig. 5.89: Q-DLTS analysis of annealed cases

Other associated trap parameters that is determined from the linearization of Equation 5.8 are trap energy level (E_T) and the capture cross-section (σ). From this whole scan, the slope of the curve provides the information of trap location (E_T) and y-intercept directs the capture cross-section (σ). The sign of trap energy levels has much importance because this provides the

information about the generation and recombination centres with-in the band gap i.e. negative signed trap (generation centre) localized near to conduction band edge and positive signed trap (recombination centre) localized near to the valance band edge. The self-explanatory energy band picture for both the implant cases along with their respective trap centres are shown in Figure 5.90.

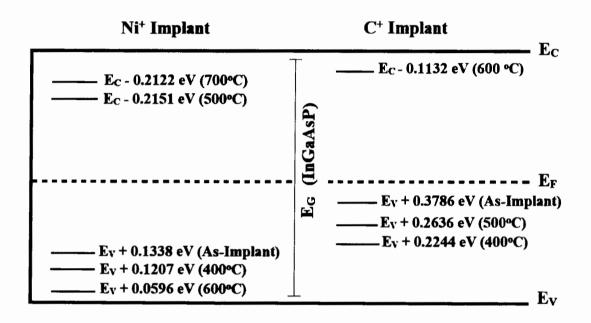


Fig. 5.90: Trap assisted energy band picture of InGaAsP after the ion implantation and post-processed annealing. It is evident from this band picture that for both as-implant cases, their trap centers are recombination ones i.e. both lies below the fermi level and the extent of level for C^+ case is far above when compared with Ni^+ ones. Another parameter which provide the strength of that specific trap center is the capture cross-section (σ). It is the ability of specific trap to capture the free charge carrier coming from their respective band edges i.e. higher the trap's capture cross-section higher will be the possibility available to trap the free carrier at said specific energy level within the band gap (signifies the quality and extent of isolation achieved within the active device region). Only this distinct information is not enough to describe the trap's role and effectiveness, all three parameters may be visualized so that the intensity of particular trap would be predicted. For instance, for as-implant C^+ , the trap location is far above i.e. $E_V +$

0.378 eV and the capture cross-section magnitude are about 6.4 x 10⁻²⁰ cm². Now, one has to see the available trap densities herewith which vary from 2.11x 10¹¹ - 7 x 10¹¹ cm⁻². For asimplant Ni⁺, the trap location is relatively near the valance band edge i.e. E_V + 0.1338 eV and the capture cross-section magnitude is about 3.1 x 10⁻²⁴ cm² with available trap densities about 1.39 x 10¹¹ - 1.18 x 10¹² cm⁻². Thus, the power/intensity of the trap centre has to be envisaged through the capture cross section. In our case, the C+ has larger capability to capture free carrier which is desirable for carrier isolation. Now the next approach to see the extent of particular trap is trap densities/concentration, which is lower for C⁺ case. This means that the trap level of E_V + 0.3786 eV has larger capability to capture free charge carrier but have lesser available states where the collected charge has to be sustained. On another hand Ni⁺ ion has relatively lesser carrier's capturing capability but have larger available states. This phenomenon has cross-witnessed from our sheet resistance analysis where the magnitude of Ni⁺ is larger when compared with C⁺ ion. Thus, this study provides an evidence that conventional transport properties may also follow these transient natures and are reliable within their scope. Table 5.8 provides a detailed account of various parameters measured from transients of charge technique for the C⁺ and Ni⁺ implanted n-InGaAsP/InP device matrix.

5.2.3.6 Transient of Photo Voltage (TPV) Analysis of InGaAsP based PIC Platform

The transient behavior of photo voltage (TPV) has also been studied where we have applied a sharp pulse of light in order to study the electro-optical behavior of all said devices. During this study the anode and cathode both electrical contacts are placed at is zero volts. This specialized configuration has adopted just to study the electrical response in order to gauge the optical drift mechanism of had InGaAsP matrix. During this analysis are fixed intensity of the same optical resource has applied in order to generate electrical charge, during this phenomena the band gap of the expectation source is same, thus, the incoming energy of excited Photon has also been fixed. Now, its up to the measurand sample that the band gap of said sample is

higher or lower with respect to the incoming excited photons energy. When these photons strike with the zero-drift potential surface, the energy of photons transfers to the stroked lattice of the sample. During this process bounded Carriers of the lattice becomes free and collected at the anode and cathode of the sample and are measured. For zero-volt drift potential, these generated Carriers are produced only for a limited period of time commonly called transients. Upon these transient the developed voltage Rises to the steady state value and the decay of the Carriers be recorded as a function of time. When the sharp light ends up then the decay of the photo voltage may also be recorded, and this value decreases up to zero drift bias (i.e. initial condition of the pre-pulsed). Photo voltage transient at the end of the light pulse consists of rapid drop followed by the slower decay. The initial drop is due to electron-hole pair recombination and the slow decay is due to carrier emission [73]. For all said samples (Ni⁺ and C⁺); the optical illumination has applied and varied the drift electrical bias and scanned the photovoltage spectra.

5.2.3.6.1 TPV measurements for C⁺ Implanted InGaAsP based PIC Platform (As Implanted and Annealed)

The TPV measurements of C⁺ implanted samples have been recorded for as implanted and annealed at 400°C, 500°C, 600°C, 700°C and 800°C at multiple drift bias, which has been varied from 0V to 5V. All the measured spectra are presented below in Figs. 5.91, 5.92, 5.93, 5.94, 5.95 and 5.96:

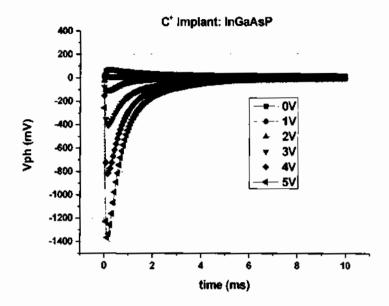


Fig. 5.91: Transient Photovoltage spectra for as Implanted C* sample

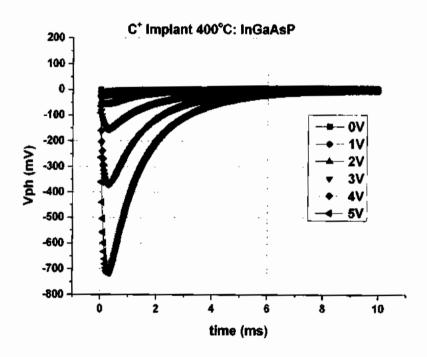


Fig. 5.92: Transient Photovoltage spectra for C+ Implanted annealed at 400°C

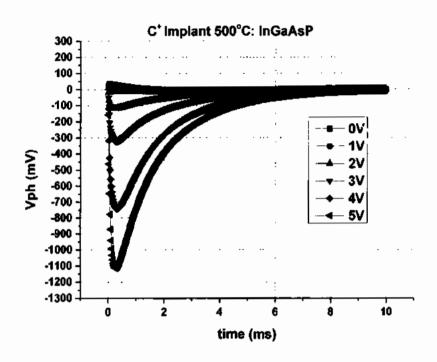


Fig. 5.93: Transient Photovoltage spectra for C+ Implanted annealed at 500°C

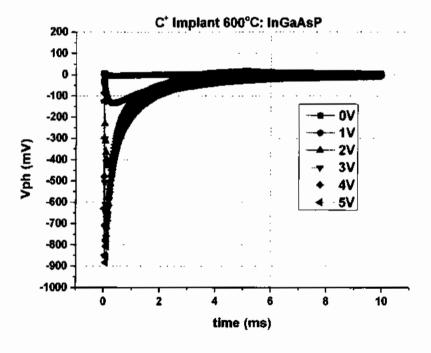


Fig. 5.94: Transient Photovoltage spectra for C+ Implanted annealed at 600°C

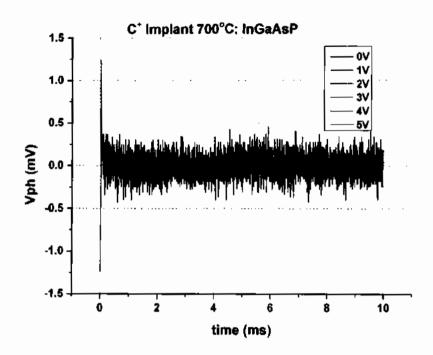


Fig. 5.95: Transient Photovoltage spectra for C+ Implanted annealed at 700°C

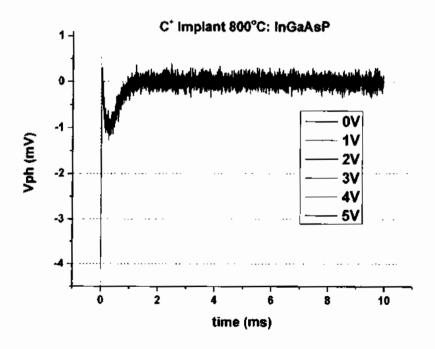


Fig. 5.96: Transient Photovoltage spectra for C* Implanted annealed at 800°C

5.2.3.6.2 Summary: TPV measurements of C+ implanted InGaAsP PIC

TPV measurements can also be used to highlight the importance of annealing process by keeping the bias constant and increasing the annealing temperature. This will reflect the amount of recovery that has occurred due to annealing. These comparative graphs can easily be generated by keeping the bias constant and reflecting the variation in spectra at different temperatures. The drift bias of zero volt and 5V applied potential have shown in Figure 5.97 and Figure 5.98 below:

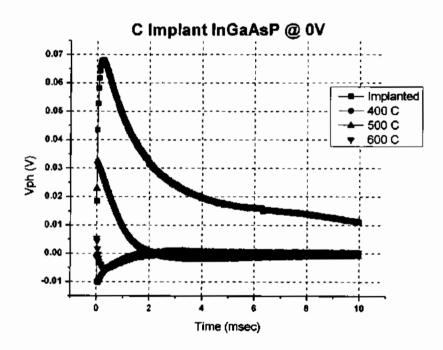


Fig. 5.97: Transient Photovoltage spectra for C+ Implanted InGaAsP keeping bias at 0V

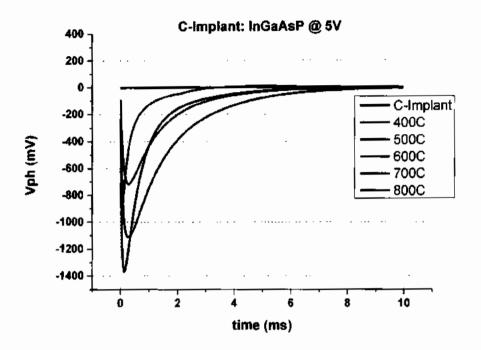


Fig. 5.98: Transient Photovoltage spectra for C+ Implanted InGaAsP keeping bias at 5V

5.2.3.6.3 TPV measurements for Ni⁺ Implanted InGaAsP based PIC Platform (As Implanted and Annealed)

The TPV measurements of Ni⁺ implanted samples have been recorded for as implanted and annealed at 400°C, 500°C, 600°C, 700°C and 800°C at multiple drift bias, which has been varied from 0V to 5V. All the measured spectra are presented below in Figs. 5.99, 5.100, 5.101, 5.102, 5.103 and 5.104:

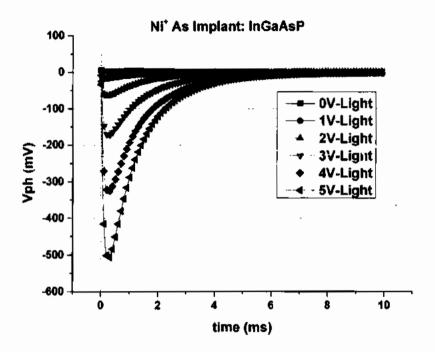


Fig. 5.99: Transient Photovoltage spectra for as Implanted Ni⁺

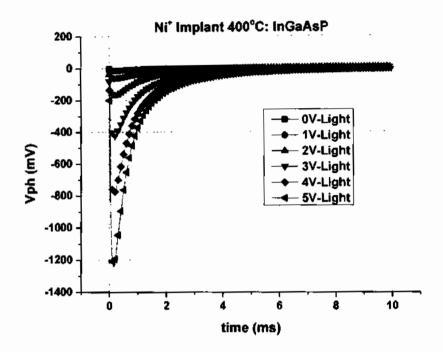


Fig. 5.100: Transient Photovoltage spectra for Ni* Implanted annealed at 400°C

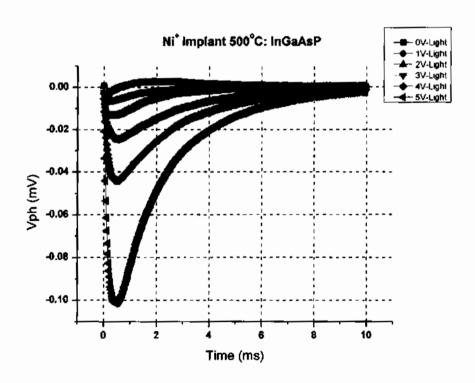


Fig. 5.101: Transient Photovoltage spectra for Ni⁺ Implanted annealed at 500°C

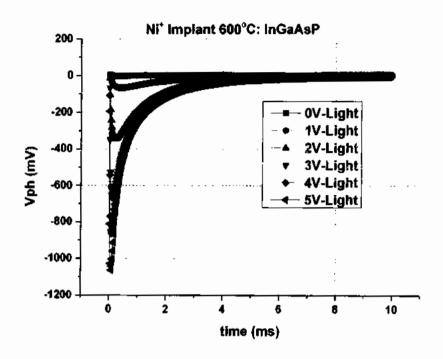


Fig. 5.102: Transient Photovoltage spectra for Ni⁺ Implanted annealed at 600°C

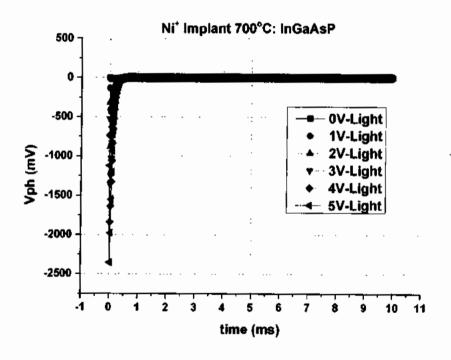


Fig. 5.103: Transient Photovoltage spectra for Ni⁺ Implanted annealed at 700°C

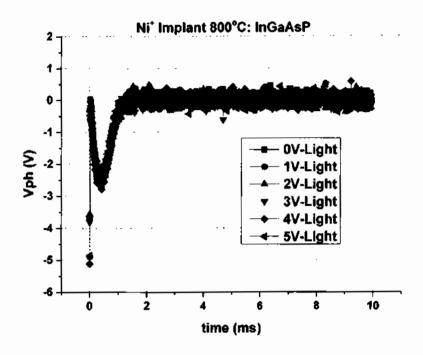


Fig. 5.104: Transient Photovoltage spectra for Ni⁺ Implanted annealed at 800°C

5.2.3.6.4 Summary: TPV measurements of Ni⁺ implanted InGaAsP PIC

TPV measurements can also be used to highlight the importance of annealing process by keeping the bias constant and increasing the annealing temperature. This will reflect the amount of recovery that has occurred due to annealing. These comparative graphs at zero and 5V (and shown in Figure 105 and 106) can easily be generated by keeping the bias constant and reflecting the variation in spectra at different temperatures.

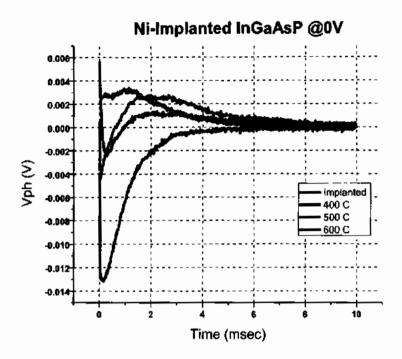


Fig. 5.105: Transient Photovoltage spectra for Ni⁺ Implanted InGaAsP keeping bias at 0V

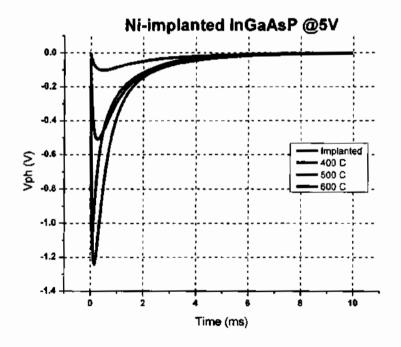


Fig. 5.106 Transient Photovoltage spectra for Ni⁺ Implanted InGaAsP keeping bias at 5V

5.3 An Overall Picture

Monolithic integrated ability in the photonic ICs has been far more beneficial when compared with their respective hybrid integration matrix. A lot of studies have been considered to develop the things in monolithic domain. In our part of study, we have fabricated two different sets of photonic integrated circuit's platforms i.e. GaN and InGaAsP and implanted them with {He⁺, C⁺}, and {C⁺, Ni⁺}, respectively; in an alternate manners. After the ion implantation, our main study was typically focused to fabricate the electrically isolated regions between surrounded conductive networks. For n-type (Si-doped) GaN; He⁺ ion was bombarded with 800keV ion energy and the fluence was about 1x10¹⁴ cm⁻². Whereas for C⁺ ion we have adopted multiimplant strategy and used single ion with multiple ion energies and dosages i.e. 2500keV, 1200keV and 800keV energies were chosen at the same ion fluence of about 1x10¹⁴ cm⁻². For InGaAsP/InP matrix; we have adopted same multi-implant strategy i.e. C⁺ ions were bombarded at 800keV and 1000keV at the ion fluence of 1x10¹⁵ cm⁻² and 1x10¹³ cm⁻², respectively. Whereas for Ni⁺ ion; we have chosen ion energies of 2000keV and 1000keV at 1x10¹⁴ cm⁻² and 1x10¹⁵ cm⁻², respectively. After the ion implantation routines, the subjected PIC platforms have been treated under multi-flux annealing routines from 300°C-1000°C and evaluated under current-voltage (I-V), transient of photovoltages (TPV), carrier transport parameter investigation using HALL effect method, charge deep level transient spectroscopy (Q-DLTS) and kinetics of dark and photocurrents, at length. Followings are few studies that have been carried out in this domain.

Jiajie Lin et al. in 2017, have worked on the electrical isolation of InP thin films for Silicon based hetero integration and used multi-energy implant. They have bombarded He⁺ and H⁺ ions on the subject lattice and evaluated the extent damage into the device matrix. For this purpose, they have chosen same sample for both of ions i.e. initially He⁺ ions were bombarded with the ion energy of 115keV and then H⁺ with 75keV. The ion fluence of He⁺ was 2x10¹⁶ cm⁻

² and for H⁺ this was taken about 7x10⁷ cm⁻² and all the physical ion implantations was performed at room temperature. After the ion implantations, they have treated the said samples under rapid thermal annealer at 150°C for surface blistering. They have performed XRD and SEM, TEM and the Arrhinias analysis of the same sample and evaluated the activation energy of 0.427eV [94].

Giovanni Alfieri et al. in 2019, have investigated the minority carrier traps in the n-GaN structure. For that purpose, they have used Be⁺, Mg⁺ and Mn⁺ multi-implant routine on n-type GaN. Initially, they have used SRIM examination tool for examining the ion distribution within the n-GaN lattice. After ion implantations the subject n-GaN matrix has annealed at 500, 800 and 1000°C for 5 minutes duration. They have evaluated the internal traps locations using the minority carrier trap spectroscopy (MCTS). They have found three trap levels within energy band picture of n-GaN matrix i.e. Ev+0.15, Ev+1.2, and Ev+0.85eV [95].

Chapter 6

Conclusion and Future Work

We have extensively envisaged the GaN and InGaAsP based Photonic Integrated platform.

The case wise conclusion and corresponding future work has been elaborated below:

6.1 Conclusion

As the possible solutions to meet the requirements of smaller footprint, lower power and costeffectiveness lies in the revalidation and advancement of technology; platform or the substrate
for photonic integration are becoming increasingly important. Silica-on-silicon, Silicon-oninsulators, III-V semiconductors such as InP, GaAs and their variants, and Lithium Niobate are
being developed and revisited for applications in monolithic as well as hybrid integration of
devices. III-V platforms have enriched the industry with their versatile applicability in
photonics. Improvement in such systems by improving the performance through reduction of
parasitic losses and physical delay lengths has been a focal point of current research in this
area. This is predominantly being done by locally modifying the character of the III-V
semiconductor (e.g., InP, GaAs, GaN or their variants) to suit the requirements of optical
components. Band-gap engineering, ion-induced engineering of devices in form of electrical
isolation, quantum-well intermixing, inter-diffusion, and impurity free vacancy disordering are
extensively been researched to propose such alteration for possible fabrication of efficient
platforms for PICs.

In this dissertation, we have keenly focused on the ion induced engineering for electrical isolation of photonically active III-V substrates. For that matter, Fabrication and their extensive characterization of III-V platforms (GaN and InGaAsP/InP) for Photonic Integrated Circuits has been envisaged, where we have used the novel combination of variety of ion-induced

engineering techniques for our device matrix. This had yielded an optimized process routine to make an all-implant strategy for a device scheme which would act as carrier transmitter and carrier isolator when exploited as a potential monolithic PIC platform under different annealing temperatures.

Based on the measurements of GaN/Sapphire and InGaAsP/InP based photonic integrated circuits (PIC) platform the key highlights of the work listed below:

- a) Initially the SRIM calculation are performed for multiple ions that have larger extent to physically damage the GaN surface. From the trajectory profiles we have performed TRIM simulations for better clarity and vacancy distributions that may leads for the establishment of ion-assisted damage into the GaN lattice. The literature suggested multiple ions to achieve the electrical isolation were H⁺, He⁺, N⁺, F⁺, Ar⁺, Mg⁺, Xe⁺, O⁺, Zn⁺, Fe⁺ and Kr⁺.
- b) From TRIM calculations we have readily focused on two different ion species i.e. He⁺ and C⁺ and used multi energies to see the extent of ion placement, damage, and vacancy profiles. From the ion trajectories, we have selected 800keV for He⁺ ion and for C⁺, have adopted multi-implant strategies i.e., three different ion energies 2500keV, 1200keV and 800keV.
- c) For He⁺ Implant scheme; the maximum concentration of ions is placed at about 2μm depth whereas same number of vacancies has generated at this particular depth.
- d) For C⁺ Implant scheme; three consecutive ion energies were taken, and their corresponding maximum depth (Rp) were around 1.15 μ m, 1.65 μ m and 2.2 μ m. From their collective response the damage profile was around 10^{14} - 10^{15} orders from the surface, which comprise maximum damage throughout the lattice.

- e) From the estimated trajectories of TRIM, the GaN deposited over Sapphire substrate were subjected under same ion implantation routines and treated at the same energies at the ion fluence of 1×10^{14} cm⁻² that have highlighted earlier.
- f) For the proper investigation; ion implanted n-GaN/Sapphire matrix were treated under electrical characterization, in order to map the extent of physical damage that had produced during ion bombardment routines. For that purpose; we have evaluated our subject matrix under Electrical transport measurements, Current-Voltage (I-V), Arrhenius Analysis, Charge deep level transient spectroscopy (Q-DLTS), Transient of Photovoltage (TPV) and Kinetics of Dark and Photo Current (I-t) analysis at multiple ambient of drift bias and luminous conditions.
- g) From Sheet Resistance analysis it has witnessed that for both of implant cases greater than $\sim 10^9 \ \Omega/\Box$ has observed, which has too significant for the optimum electrical isolation and damage of the parent lattice because the original lattice of n-GaN matrix has $16.9 \ \Omega/\Box$.
- h) It is gathered that persistence of isolation achieved in the substrate matrix is strong enough not to let the movement of even fewer numbers of free carriers within the free device region.
- i) After initial assessment, both of the ion induced in n-GaN matrix have been treated under 300°C-1000°C and evaluated the same characterization as described above.
- **k**) The activation energies (E_a) analysis has been performed for all annealing cases and inspected that He⁺ implant case provides maximum damage which eventually declares maximum energy to the free charge carriers that may produce conduction. For better electrical isolation, the activation energy has to be as high as can be achieved. For all, He⁺ provides the asymptotes when compared with C⁺ Ion. While annealing dynamics; this phenomenon can he attributed towards the bonding capability of the incoming specie with the host lattice that may contribute extra charge migration and contribute larger electrical conduction. For C⁺ case it has high tendency available to bond with the parent lattice's atoms i.e., Ga or N, at rather higher

annealing temperatures. But for He⁺ ion, there is absolutely no chance for subject bonding phenomena because of its inert nature i.e., completely filled valance band.

- I) In order to map the photo response of both available PIC platforms, we have evaluated the photovoltaic as well as photoconductive response for each implant strategy. For photo-voltaic; no external drift bias has been applied on both sets (He⁺ and C⁺) of PIC and just photons (@179000lux intensity) have been shined and measured the electric current at zero applied bias. For He⁺ case 700°C and for C⁺ case 500°C annealing temperature was more favorable that provides an optimum rectification ratio i.e., I_{ON}/I_{OFF}. For photo-conductive topology; an external drift bias has been applied and recorded the same rectification ratios. Whereas at 900°C and 1000°C annealing temperature no physical attribute (difference) has been observed in electric current magnitude i.e. same currents are recorded for Dark and luminous conditions.
- m) To map the photo transients, we have frequently evaluated the transient of photovoltage (TPV) measurements at 0, 1, 2, 3, 4, and 5V drift biases. After the careful examination it was observed that for, He⁺ implant matrix 300°C is more favorable and for C⁺ case 500°C annealing temperature is most favorable that contribute larger extent of photovoltage that is necessary for the detection of available light and hinder the electrical transport in terms of charge migration through the implanted ones.
- n) A very sophisticated technique based on the measurements of transient of charges named Charge Deep Level Transient Spectroscopy (Q-DLTS) has been performed on He⁺ and C⁺ implant cases. This study has been utilized to investigate the traps centers and their characteristic parameters i.e. Trap Location within the Energy band picture (E_V+E_T or E_C-E_T), Trap densities (N_T) and the associated capture cross section (σ) that provide the power of the trap i.e. how much that specific trap center is capable to trap the free carrier from their respective band edge.

- o) Likewise, GaN; Molecular Based Epitaxy (MBE) InGaAsP PIC platform has been initially simulated at multiple ions i.e., H⁺, He⁺, B⁺, N⁺, O⁺, F⁺, Fe⁺ and Ga⁺ ions have been reported in literature on the modelled on the Monte Carlo based software package SRIM. After the careful investigation of the ion trajectories of SRIM calculations we have chosen C⁺ and Ni⁺ ions with the multi-implant strategy i.e., multiple times of same ion but with different energy and fluence have been utilized for both of such cases. For C⁺ ion 800keV and 1000keV ion energies and for Ni⁺ 1000keV and 2000keV ion energies were chosen and investigated the ion distribution, vacancy profiles, projected range, backscattered ion count and transmitted ion profiles in a very minute details before their selection.
- p) On the basis of TRIM calculations, we have performed physical ion implantation at the same energies i.e. For C⁺ case; 800keV (ion fluence of 1x10¹⁵ cm⁻²) and 1000keV (ion fluence of 1x10¹³ cm⁻²) and for Ni⁺ case; 2000keV (ion fluence of 1x10¹⁴ cm⁻²) and 1000keV (ion fluence of 1x10¹⁵ cm⁻²), were chosen energy after energy at the prescribed ion fluence.
- q) After the physical ion implantations InGaAsP based PIC matrix were treated under same electrical characterization that have been performed for GaN PIC matrix i.e., Current-Voltage (I-V), Arrhenius Analysis, Charge deep level transient spectroscopy (Q-DLTS), Transient of Photovoltage (TPV) and Kinetics of Dark and Photo Current (I-t) analysis at multiple ambient of drift bias and luminous conditions. These all measurements have been taken at multiple annealing temperature ranging from 400-800°C.
- r) From sheet resistance analysis, this was observed that initially Ni⁺ has comparatively larger tendency of carrier loss mechanism and provide of the order of $\sim 10^6 \,\Omega/\Box$, whereas C⁺ has $\sim 10^5 \,\Omega/\Box$. Although at 400°C and 500°C both ions provide same amount sheet resistances but their internal field dynamics were far away from each other that have been measured by other experimental verification techniques.

- s) The sheet carrier mobility analysis has provided the information that C⁺ ion has lesser mobility when initially bombarded with the host InGaAsP lattice. Although next upcoming annealing temperatures suggests entirely changed graphics into the whole picture.
- t) The activation energy analysis on parent InGaAsP PIC matrix was around -0.026eV whereas for as Ni⁺ and C⁺ as implant cases; -0.15eV and -0.65eV, energies were required. This analysis has also proven that for as implant C⁺ ions have higher approach towards electrical isolation because higher magnitude of activation energies means larger energies are required for the electrical conduction through subject design matrix.
- u) The detailed Q-DLTS characterizations have performed and localization of multiple charge trap centers are evaluated and identified that may provide the color and hinderance centers to the incoming photons and electric charge, respectively. Also, the trap measurements provide an insight at an atomistic level by which one can easily determine the recombination and generation centres for potential photonic activity at device operational level and provides cross evidence that conventional transport properties also follow these transient natures and are reliable to ascertain the electrical isolation for photonic circuits.
- v) The TPV measurements have performed at 0-5V at same spike of light intensity, and it is observed that for Ni⁺ implant case 400°C annealing temperature is more favourable and for C⁺ the only as implant case provide maximum transient of photo-voltage.
- w) A detailed analysis of kinetics of currents have also been investigated at multiple annealing temperatures and biases.
- x) In totality, the fabricated substrates i.e., GaN/sapphire & InGaAsP/InP subjected to carefully selected isolation implants and annealing windows provide a sufficient evidence to be utilized as platform for both active and passive components for PICs development. This is confirmed by virtue of isolation characteristics duly verified by several detailed characterization analyses

in this study. This is also evident that one may utilize these device structures as blockers/isolators or transporters of free carries needed to actively design various portions of substrate used in PIC fabrication. The schemes presented in this work have ramifications for both device designers and photonic processing engineers.

6.2 Future Work

In future perspectives the multiple inert ions may have to be chased for the optimum evaluation of larger extent of damage into the photonic integrated circuits (PIC) platform. In this study we have chosen relatively larger extent of implant energies that have produced the damage extent surface and into the bulk. For futuristic approach, one can exhibit low level energies with He⁺, H⁺, Ni⁺ and C⁺ ions with low implant to only damage the surface that may provide larger extent of damage only on the surface rather than on bulk.

- a) Integration of active (transmitter, receiver) and passive (waveguide) onto a single chip can be fabricated onto a single IC platform which can act as a standalone system on a chip platform that have capability to process both optical and electronic signals into a time and frequency division domain signaling transceiver. For that purpose, GaN is most favorable photonic integrated circuit (PIC) on a GaN-on-sapphire platform.
- b) A comprehensive TEM analysis has been needed for each GaN and InGaAsP platform. From this approach ultra-shallow junctions (UHJs) near the interface level of ion induced region can be actively utilized for active as well as passive set of approaches.
- c) GaN based PIC platform can be utilized after the keen full investigation of next generation i.e. more than 12 THz regimes because 5-12 THz regimes GaN are working in robust manners.
- d) From above approach, GaN is one of the most promising semiconductor materials for the next generation THz emitters, detectors, mixers, and frequency multiplicators on a single node

of PIC wafer. From this topology GaN-based electronic devices may including plasma heterostructure field-effect transistors, negative differential resistances, hetero-dimensional Schottky diodes, impact avalanche transit times, high electron mobility transistors, quantum-cascade lasers, Gunn diodes, and tera field-effect transistors together with their impact on the future of THz imaging and spectroscopy systems.

- e) GaN has also tendency to radiate light, thus can be utilized for radiating the photons up to 3.4 eV energy domain. Also, the lower energy photons can be emitted and sensed by introducing multiple color centers using low energy ion implantation.
- f) InP has ample amount of opportunities available due to its monolithic capability that proves it an advanced photonic integrated platform which can process photonic signals as transmitter, receiver, and blocker at the same platform.
- g) Virtuoso Schematic Editor XL and TCAD SilvacoTM can also be utilized for next generation PIC technology because the concerned TCAD vendors continuously improve their libraries for futuristic research.

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