Hypersensitive Electrical Characterization of 2D Graphene Transistor Matrix

MS Thesis

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Session 2013-2016

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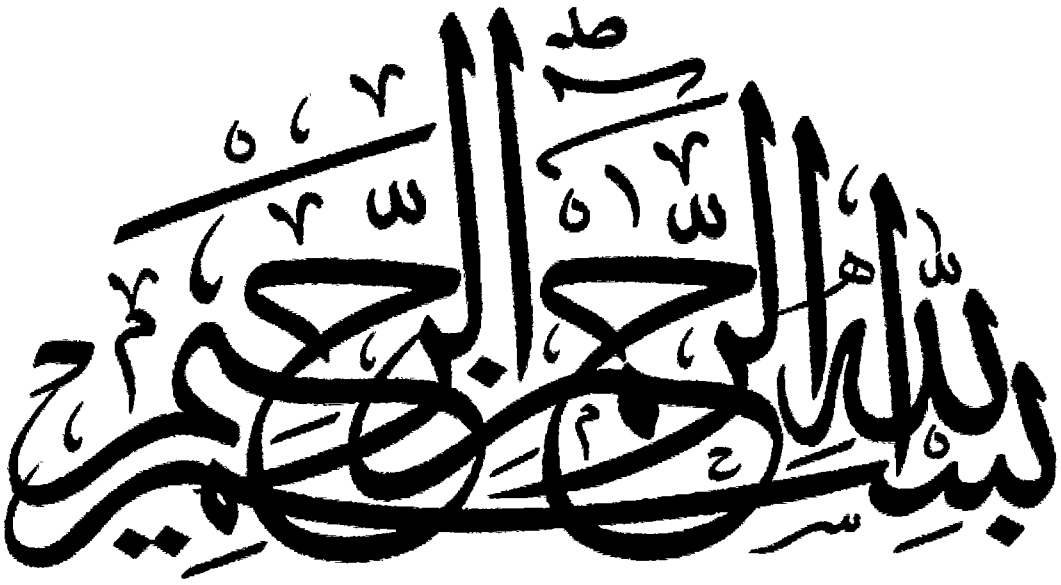
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Hypersensitive Electrical Characterization of 2D Graphene Transistor Matrix

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331-FET/MSEE/F13

Submitted in partial fulfillment of the requirements for the

Master of Philosophy degree in Electronics Engineering with specialization in Advance Electronics at the faculty of Engineering and Technology department of Electronic Engineering International Islamic University Islamabad

Supervisor:

Day, Month, Year

Title of Thesis: Hypersensitive Electrical Characterization of 2D Graphene Transistor Matrix

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Viva Voice Committee:

Dean

Chairman/Director/Head

External Examiner

Supervisor

Member

(Day, Month, Year)

DEDICATION

This Thesis is dedicated to my

Beloved Parents

And

My Friends

Certificate

This is certifying that the work contained in this thesis entitled:

"Hypersensitive Electrical Characterization of 2D Graphene Transistor Matrix" been carried out by ***Shah Fahad*** under the registration ***331-FET/MSEE/F-13*** in Advanced Electronics Laboratories under my supervision. In my opinion, this is fully adequate in scope and qualifies the degree of the MS Electronic Engineering with specialization of the Advanced Electronics.

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1.1 Introduction:

In 1965 the co-founder of Intel Gordon E Moore published a paper around six years after the invention of first integrated circuit by Robert Noyce, by the title 'cramming more components on to integrated circuit' in which he predicted that the numbers of transistors inside a chip will become double every two years [1]. Moore's law was a guideline for semiconductor industries to achieve their future targets and long term planning. Construction of a semiconductor device needs a lot of operation like photolithography, etching, and metallization, so to perform these operation industries need the most advance and sophisticated machine made by commercial companies worldwide. Now for new advancements in these commercial designing tools, the semiconductor industry association USA, Japan, UK, South Korea and Taiwan led the foundation of International Technology Roadmap for Semiconductors (ITRS) in 1998. The last ITRS roadmap was published in 2013 in which the nodes are defines for future technology [2].

Year	Node	Year	Node	Year	Node
1971	10 µm	1995	350 nm	2010	32 nm
1974	6 µm	1997	250 nm	2012	22 nm
1977	3 µm	1999	180 nm	2014-15	14 nm
1982	1.5 µm	2001	130 nm	2016-17	10 nm
1985	1 µm	2004	90 nm	2018-19	7 nm
1989	800 nm	2006	65 nm	2020-21	5 nm
1994	600 nm	2008	45 nm		

Table 1.1: ITRS roadmap for current and future technology.

In table 1.1 the node means the size of transistor gate or we can say that the industry has the capability to pattern the desire length structure by photolithography. For complete details of the device shrinking Intel had presented a Tick-Tock model adopted by chip manufacturers [3]. In table 1.1 the node 10 nm is known as beyond CMOS technology and is not a silicon based technology because the physical limits of silicon prevent it further miniaturization. As a CMOS transistor function involved both holes and electrons as a charge carrier but as we know that holes mobility's are very low in silicon as compared to electron. Next is the heating issue because the performance of silicon degrades at high temperature while the alternative material like gallium nitride Silicon carbide and graphene perform well at high temperatures and does not require a heat sink. The most important issue related to silicon transistor is that upon further miniaturization the silicon dioxide loses it insulation properties.

So to keep Moore's law alive chip manufacturing industries are going to shift to the post silicon technologies but the question is which new material is the best contender to replace silicon. The ITRS have suggested two types of solutions, a short term solution and a long term solution. The short term solution is to replace silicon CMOS technology with Ge and in GaAs or All Ge CMOS technology. The long term solution is to replace silicon or the materials in the short term solution with CNT (Carbon Nano Tube), Graphene, TMDC (Transition metal di-chalcogenide). In this thesis we are going to explain the long term solution because our projects are based on graphene transistor structure. Graphene is a single sheet of carbon in honeycomb lattice structure and is a good conductor of heat and electricity. The electron mobility of graphene is 100 times greater than silicon [4]. Single sheet of graphene is thermodynamically stable at room temperature while the miniaturization in silicon is the

main issue. Graphene based transistor can be used for Tera Hertz transistor application as IBM has already graphene based front end receiver which operates at 4.3 GHz. The main issue related to graphene is the compatibility with other material because graphene's to much high conductivity is difficult to handle.

1.2 Thesis Motivation:

Graphene is the 2D, single atom thick sheet of hexagonally arranged carbon atoms and is the basic building block for carbon nanotube and fullerenes. Graphene was discovered by two scientists Andre Geim and Konstantin Novoselov at the University of Manchester in 2004 and get Nobel Prize in physics in 2010 [5]. Graphene is a Novel material also known as the material of the century due to its extra-ordinary and magical properties. According to Dirac equation the relativistic mass of charge carriers inside a graphene is zero and can travel with a speed nearly to the speed of light that is why these charge carriers are called the Dirac fermions. Graphene has exceptional and the most unique electrical, optical and mechanical properties. Mechanically graphene is 100 times stronger [6] than steel with breaking strength of 43- Nm and with elastic limit of 20% [7] means that it can be stretched 20% more than its original shape without any damage. The most important property of graphene is its highest electron mobility of 200,000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [8] at room temperature 100 times greater than silicon and the carrier density of 10^8 A/cm 100 times more than Cu. Graphene is optically transparent and absorb only 2.3% of light and also the lithest material by weight as only a gram of graphene can cover a whole football ground.

Now the most considerable thing is that graphene is the most sensitive material and all of these properties changes when graphene becomes in interface with other materials like

metals and dielectrics. In case of metal interface, the modification in properties of graphene occurs duo to charge transfer, change in band structure and also due to re-hybridization. Also in case of Ni magnetization may produce in graphene and can create tunneling effects. The interface between metal and graphene depends upon the metal degree of interaction and its structure and the minimum inter layer distance between them after interaction. For strong bonding the inter-layer distance should be less than 2A° [9] as in case of Ni also for charge transfer the work function may play a key role. The most important thing is the lattice mismatch between the underlying metal and graphene. Nickel and graphene possess relatively the same lattice constant so Ni and graphene makes a hypersensitive interface. The device structure we are using in our research is grown by CVD method and have the following parameters shown in Figure 1.1:

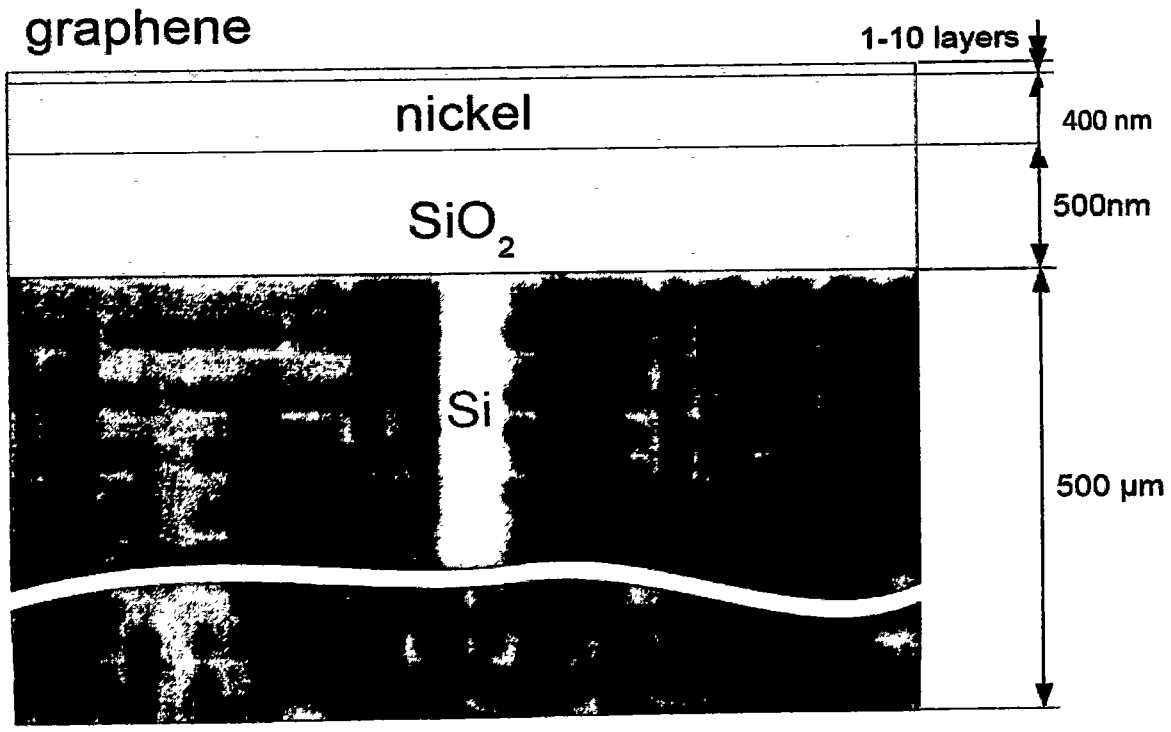


Figure 1.1: graphene transistor matrix structure.

Wafer size= 100 mm

Graphene thickness= 1 to 10 layers

Wafer orientation of Si= (110)

Ni layer thickness= 400 nm

growth method =CVD

wafer thickness =500 um

SiO_2 layer thickness=500 nm

The device structure mentioned above is known as "Graphene Transistor Matrix" and can be used for variety of graphene based transistor application when fabricated on silicon substrate. The choice of graphene layer interface with nickel (400 nm) is developed in such a way to study the hypersensitive interface electrical characterization for exfoliation in making future graphene based transistor protocol. The detailed hypersensitive electrical characterization may be able to provide us an insight to this customized transistor matrix for its utilization during graphene transistor fabrication. The problem is to identify the potential of this design structure in the applicability of few layers of two-dimension graphene transistor fabrication with lesser processing and engineering steps.

Chapter 2: Graphene Background and Theory

2.1 Graphene History:

Graphene known as a miracle material is the 2D allotrope of Carbon and the world's thinnest material ever known to mankind. Graphene is only one atom thick and considered to be the strongest material ever imagined. Its 2D nature can also be proved mathematically and when it is stretched it looks like a chicken wire.

Graphene is impermeable means that upon warming its shrinks and expands when cold, made from the ordinary Graphite as the led used in our pencils. The word graphene is nomenclature as Graphite and -ene [10] as a suffix named by the German Chemist H.P Boehm in 1962. P.R Wallace in 1947 was the first who explored the mystery of this wonder material theoretically by understanding the 3D Graphite electronic properties through the massless fermi Dirac equation.

In 1948 [11] the first ever TEM image of few layers of Graphite were published by G. Ruess. A few years later the single layer Graphene was directly observed by Electron Microscopy. In 1990 the researchers start to mechanically exfoliate the graphite thin films flakes and up to 2004[12] they were close to have 50 to 70 layers thick Graphite flakes. In 2004 two scientists at the university of Manchester Andre Geim and Kostya Novoselov [13] used bulk Graphite to extract monoatomic layers of graphene and transferred them onto SiO_2 /Si substrate using the micromechanical cleavage also known as the scotch tape method. Graphene synthesized by the cleavage technique led the foundation to the direct observation of quantum Hall effect in Graphene, which provides the evidence of massless Dirac fermions theoretically predicted.

Adre Geim and Kostya Novoselov received the Nobel Prize in Physics in 2010 for their groundbreaking experiments and pioneer research in 2D materials [14]. It is so hard to produce Graphene large sheets but now a days many new emerging production techniques has been developed such as CVD (chemical vapor deposition), roll to roll method, nanotube slicing and production through electrochemical method. Since 2004 after the extraction of Graphene from the bulk Graphite there is an explosion in terms of Graphene production methodology, characterization, extraordinary properties as well as potential industrial application.

2.2 Graphene structure:

Graphene is two-dimension crystalline form of carbon. In the hexagonal pattern the carbon atoms are densely packed with separation of 1.42 Å [15]. Each carbon atom with four electron forms 3 sigma bonds with its neighbors and the remaining one electron makes Pi bond which is out of plane and makes Electron Sea.

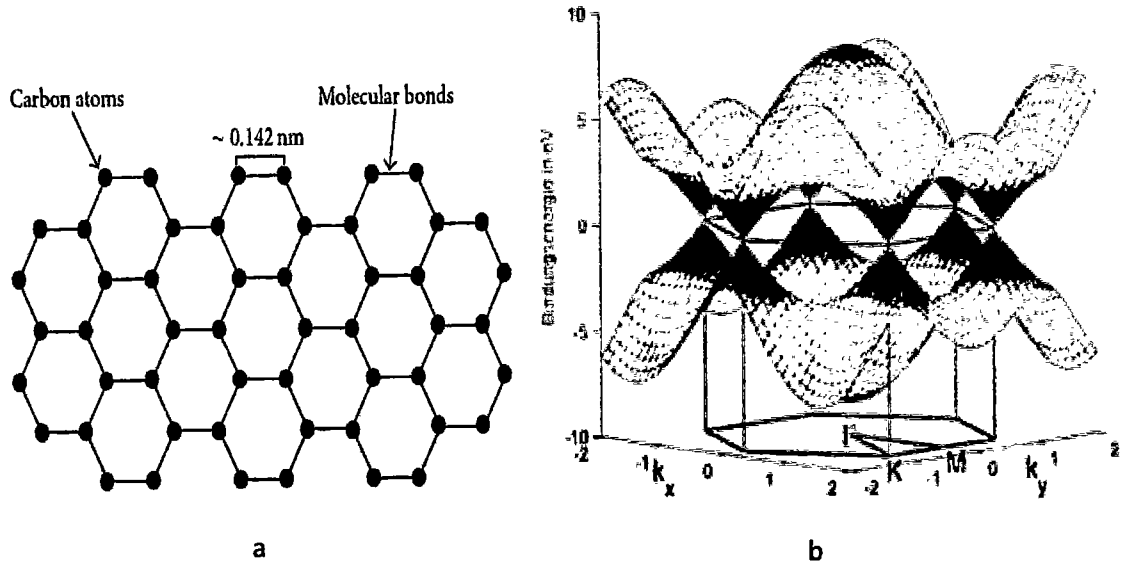


Figure2.1: (a) graphene hexagonal structure (b) band gap representation of graphene

Graphene is stable in 2D form due to the sp^2 hybridization in which 2 electrons in the carbon atom occupy the 1S spherical shell while the remaining 4 electrons are accommodated in the 2S and 2P shells. Sp2 hybridization is obtained by the hypothetical mixing of 2S and 2P orbitals. The 4^{th} electron has occupied a P orbital perpendicular the plane which makes an electron cloud that is why graphene have the ballistic charge transportation property. In graphene due to its 2D nature every carbon is available to contribute in chemical reaction and also in all allotrope of carbon graphene has the maximum ratio of edge atoms. Scientists reported that as compared to multi-layer graphene the single layer of graphene is 100 times more reactive [16].

Graphene is semi metal with zero band gap and its valance and conduction band overlaps at Dirac points at the edge of Brillouin-zone as shown in Figure 2.1. Graphene sheet is a 2-dimension membrane in a 3-dimension space so there is more configuration like, by stacking many sheets on top of each other forms graphite which is a 3D form of carbon allotrope. These layers are stacked together by a force called the Van der Waals which interacts weakly. Similarly, by rolling the graphene sheets in to the cylindrical form we can get a carbon nanotube, the 1D cousin of graphene and they both shares some of the most extra-ordinary properties of graphene. There are many more like rolling the graphene sheets into a spherical shape called Buckminsterfullerene and the Fullerenes the 0D cousin of this wonder material graphene.

2.3 Moore's law:

In 1965 the co-founder of Intel Corporation Gordon E. Moore stated a very famous law known as Moore's law which states that the total number of transistors or electronic

components in a dense Integrated circuit doubles every 2 years and the rate will be continuing for at least a decade [17]. These predictions were described in his paper "Cramming more components onto integrated circuits" published on 19 April 1965[18]. Moore's prediction proved accurate for many decades and also used for future planning to set targets for advancements in semiconductor industry developments and research. Moore's law is some kind not a physical law because the growth rate predicted by Moore held steady from 1975 up to 2012 and was faster at the first decade 1965 to the end of 1975. There is also a modified version in which instead of two years the performance of integrated circuits would double every 18 months. This modified version of Moore's law was presented by the Intel executive David House in 1975[19]. The ITRS (International Technology Roadmap for Semiconductor) investigated in 2010 that the rate would be too slow at 2013 and onward and probably 2015 will be the year of saturation of Moore's law.

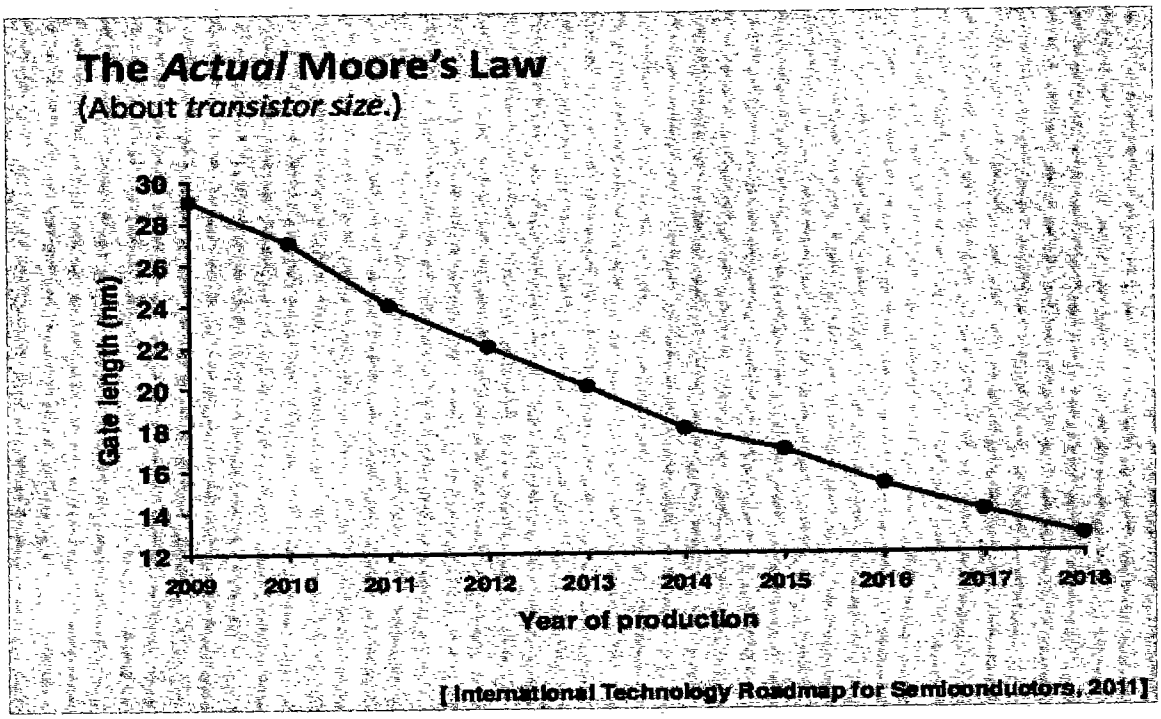


Figure 2.2: Transistor gate length vs year of production by ITRS

In 2012 and onward we have a 22nm architecture but Intel announced that at the end of 2016 they will have a 14 nm processing architecture in the market and at the mid 2017 the will be able to release a 10 nm processing chips based technology. IBM also claimed that they had created a 7nm transistor based chips and will soon be in market for competition. But the most important thing is what will be beyond 7nm and what will be the future of the Moore's law [18-19]. There are many aspects but in these thesis only the topic related problem and solution will be under consideration and will be briefly discussed in the next topic silicon vs post silicon technology.

2.4 Silicon vs Post-Silicon Technology:

After the magical prediction of Moor's law, the competition to miniaturize the device size raises new and some serious challenges for semiconductor industries. Silicon based MOS transistors ruled the semiconductor industry up to past 50 years, but the Moore's law also stated that one day we will reach the limits of transistor to function as a transistor because the physical dimensions of silicon based transistor makes it impossible to optimize its behavior and we have to attain an optimum between gate leakage current and device performance. Scaling down of silicon based transistors around 7 nm are more difficult and need to be so expensive technology to fabricate at the industry level as shown in Figure 2.3 which shows the future of current trends in developments of Intel processing node technology [20].

Digital computing is totally based on the ON and OFF concept called the binary representation and these states are the main theory behind the transistor to function like a switch. The basic issue with the silicon based transistors is that upon scaling down to 7 nm

the transistor is set to be so close to each other's so they may be effect each other's functionality due to the Quantum Tunneling effect which means that this interference will make the transistor's to stay always in the ON state, so the processing will be against the fundamental concept of digital computing.

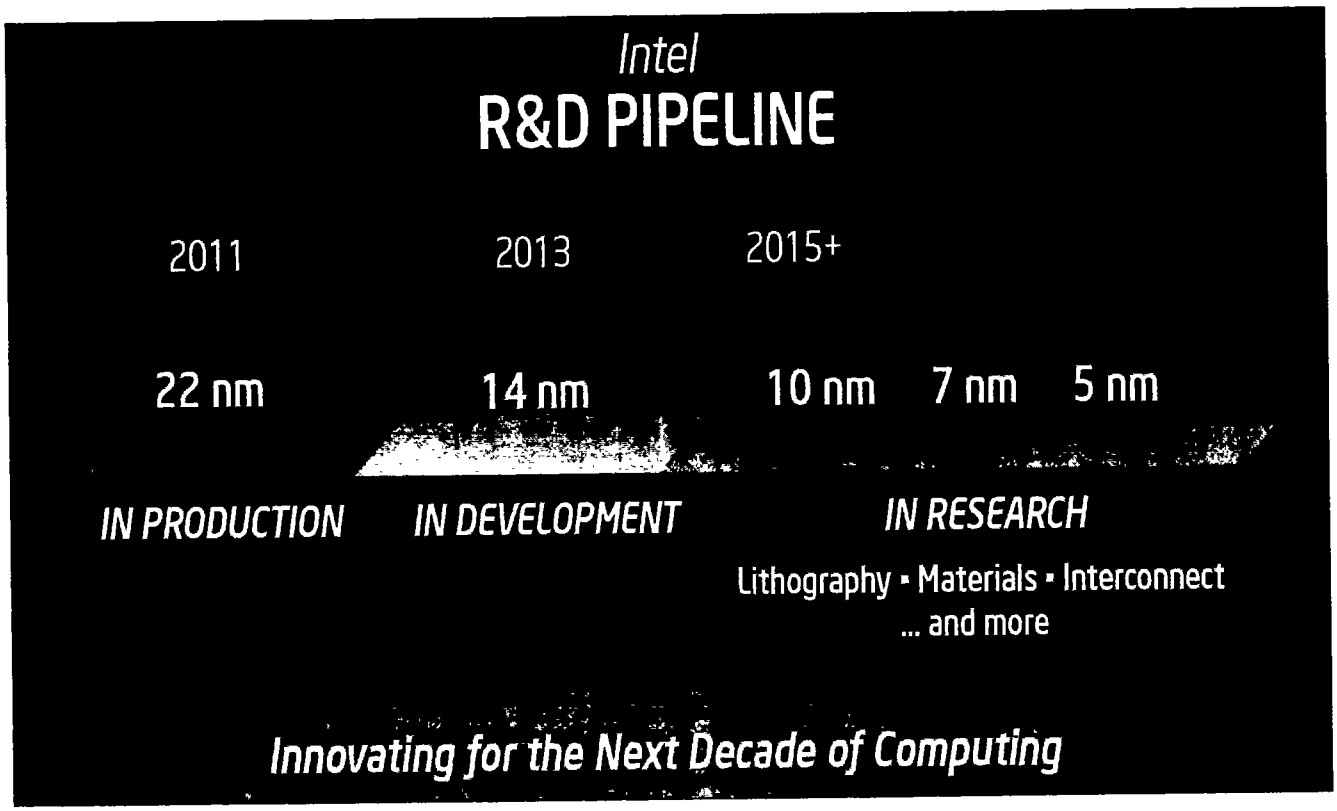


Figure 2.3: Intel Abandoning Silicon with 7nm and Beyond – Silicon Alternatives Coming by 2020

So 1st solution is to find an alternative material which could be scaled down and also have the fastest switching speed. The 2nd solution is the optical regime. The choice of alternative material is straight forward mean to find a new material which could be scaled down but also be fabricated using the standard silicon manufacturing technology. The solution to alternative material are composed of two types.

2.4.1 Short term solution:

The basic idea behind the short term solution is to find a new material having some identical properties like silicon and can be fabricated using the current technology. The most promising material to supersede silicon for next few years is group III-V semiconductor. These are four elements in the form of compounds in which one is (In GaAs) indium gallium Arsenide the other one is (InP) indium phosphide.

IMEC (International Medical Equipment's Collaborative) are given a task by leading semiconductor manufacturing companies like Intel, TSMC, IBM and Samsung to find the next thing after silicon, and they had already fabricated a Fin FET by using In GaAs and InP.

2.4.2 Long term solution:

The long term solution is to find a new material as well as a new emerging fabricating technology. Now a day's many researches are working on the two-dimension material after the invention of Graphene in 2004 which is the 2D allotrope of carbon. Graphene is more stable and the strongest material on the face of earth which the reason that the semiconductor industry is so interested in it. This is due to some extra-ordinary properties of graphene which will be discussed in the next topic "Why Graphene".

2.5 Why Graphene?

Graphene called the substance of 20th century also known as the new silicon. The question arise here why graphene is important; the answer is graphene possess some extra-ordinary properties which makes graphene so important to replace the current semiconductor

material like silicon because it is for better than silicon. Here we discuss some magical properties of graphene and compare it with silicon.

- Graphene is 2D while silicon cannot be sliced to 2D form because it becomes unstable while graphene is stable in 2D form
- Graphene is good conductor of heat as well as the electric charges while the silicon is not the good one compare to graphene
- Graphene is 97% transparent while the silicon is not
- Graphene is flexible and can be rolled while silicon is fragile
- Electron mobility of graphene is 200 times greater than silicon
- And the most important is that graphene is not limited to only semiconductor industry graphene has a variety of application almost in every field of modern technology present.

The above listed properties and there are many more makes graphene so important that one-day graphene will replace silicon and will make the chances for the survival of Moore's law.

2.6 Graphene roadmap 2020:

In October 2013 142 partners from 23 countries across the world sit together to form Graphene Flagship. Graphene Flagship was established by the European commission to find long terms solution to current challenges like big data systems. The findings are published in the research journal Nanoscale and have given open access to it [21]. This paper is the contribution of more than 60 academics and industry to find science and technology roadmap for graphene as well as other related 2D materials and also graphene based 2D

materials composites. The graphene roadmap covers the next decade and beyond as shown in Figure 2.4.

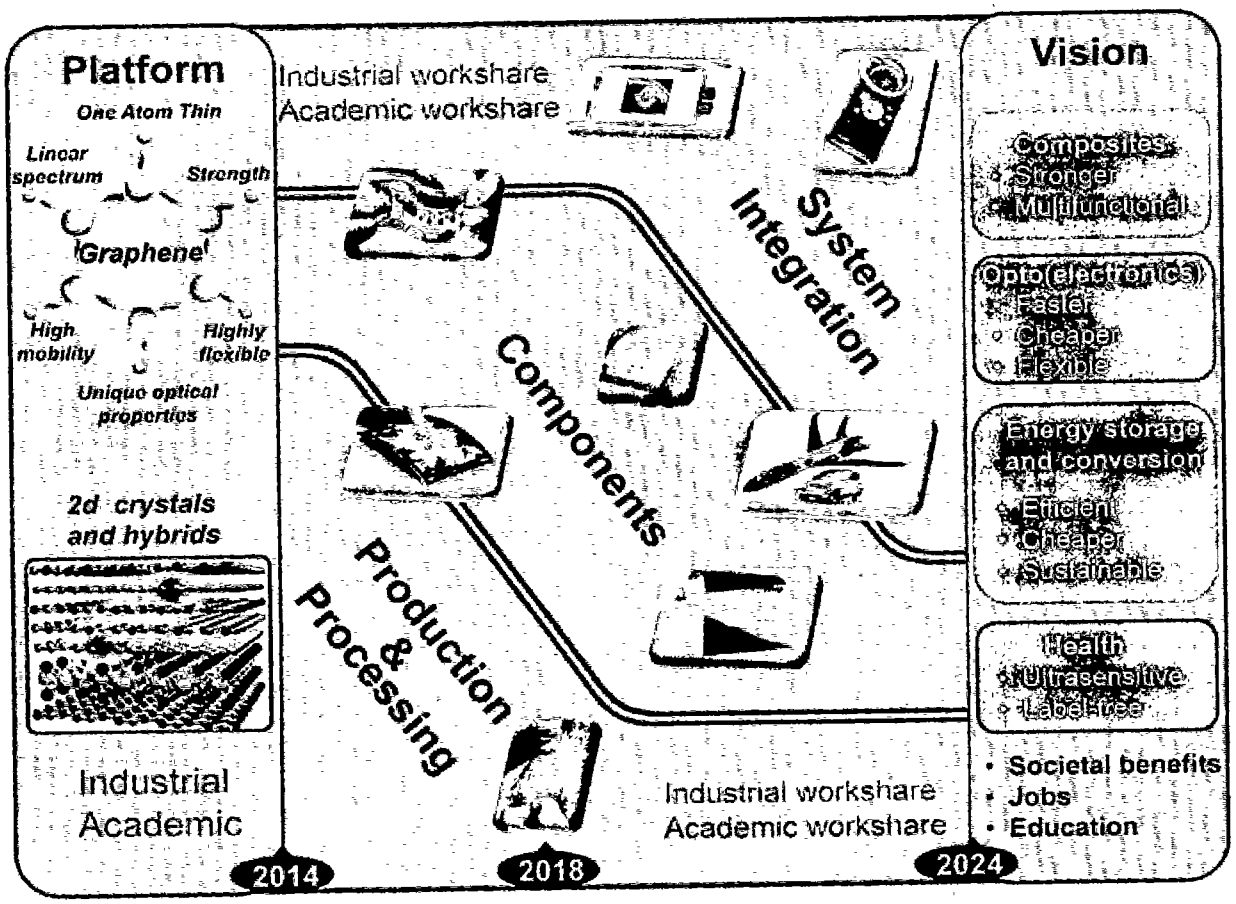


Figure 2.4: Europe's Graphene Flagship technology roadmap, targeting research areas designed to take graphene and related 2d composites from academic institutions into society

The main goal of graphene flagship is to provide guidance to industrial and community research to develop graphene and related 2D materials based products. The graphene roadmap is divided into three broad areas.

(1) The 1st task is to find new 2D material, study there potential in developing new technology and the production of these material at industrial level.

(2) The 2nd task is to identify the concept of new devices and the components which will be utilized GRM's like graphene based high frequency electronic transistors for RF application, graphene spintronic and optoelectronics.

(3) The 3rd task is system integration means to bring GRM's based new components and structure them to form a system which would have the capability to provide new application areas such as energy application and flexible electronics.

2.7 Graphene Extraordinary Properties:

Before the isolation of graphene in 2004, on the basis of theoretical formulation is was believed that due to thermal instability it is impossible for two dimension compounds to remain stable at room temperature. But from the isolation of single layer of graphene from bulk graphite is possible because graphene is single sheet of carbon and it is stable at room temperature in its 2D form. Research suggests that the reason behind graphene stability is the smallest and the strongest bonding between carbon atoms which prevents it from destabilization. Here we are discussing some extra-ordinary properties of graphene related to our research scope.

2.7.1 Electronic Properties:

Graphene is zero overlapped band gap semi metal in which both the electrons and holes are charge carriers. Every carbon atom in graphene hexagonal structure have a free electron available for charge transportation and also the effective masses of both the charge carriers are zero called the Grapinos or Dirac fermions.

Experiments show that the electron mobility of suspended graphene is 15,000 cm^2 /V. S and remain the same with span in temperature form 10K to 100K. Theoretically predicted

electron mobility of graphene is 200,000 cm^2 /V. S at room temperature which is 10×10^6 times higher than copper. Sheet resistance of graphene is in the order of 10^{-6} Ωcm less than silver [22]. The most important electrical property of graphene is that at room temperature the electron in graphene 2D structure can covers a micrometer distance without any collision, this phenomenon is called the ballistic transport of charge carriers. Graphene can also be doped to engineer the bandgap for some desired application.

2.7.2 Mechanical Strength:

Graphene is the strongest material ever known to mankind, this is due to the strongest C-C bond with a very small separation of 0.142 nm. The tensile strength of graphene is 130 GPa as compared to structure steel having 400 MP [23]. Not only graphene is the strongest material but it is the lightest material also as 0.77 mg/cm^2 which means that graphene is 1000 times lighter than paper sheet, and the most dramatic thing is that a single gram of graphene by size can cover a whole football ground. Graphene is flexible too having the Young modulus of 0.5 Tpa and the spring constant of 1-5 N/m.

2.7.3 Optical properties:

Graphene is 97% transparent material and absorb only 2.3% of white light if it is only the single sheet. Graphene due to its fine structure if we add another layer its optical properties remain the same. The opacity of graphene $\pi\alpha$=2.3% and in the visible frequency range its optical conductivity G= G=e2/4$\hbar$ (±2-3%).

Upon laser illumination intensively Kerr effect happen in graphene with a nonlinear phase shift and the Kerr coefficient of 10^{-7} $cm^2 \cdot W^{-1}$. Kerr effect in graphene determines the nonlinear effects as a medium in which the most important is Soliton [24].

2.8 Graphene synthesis

There are many well-known techniques by which we can create graphene single layer or mono layer graphene, only names of these techniques will be discussed here because in our research the graphene we are using is grown by chemical vapor deposition method so the main focus will be one CVD method for graphene synthesis.

Before going to brief details of CVD method here we have listed some other techniques through which we can create graphene.

Mechanical exfoliation	**Molten salts**
Sodium ethanol oxide pyrolysis	**Hydrothermal self-assembly**
Electrochemical synthesis	**Nanotube slicing**
Roll-to-roll	**Carbon dioxide reduction**
Spin coating	**Supersonic spray**
Graphene synthesis by laser	**Microwave-assisted oxidation**

Table 2.1: synthesis techniques for graphene.

2.8.1 Chemical vapor deposition:

Chemical vapor deposition is mostly used for growing graphene using transition metal substrates like Ni, Cu, Pd, Ru because it is the most inexpensive and the most promising approach w.r.t to cost and quality of graphene. Figure 2.5 shows the steps involves in production of graphene using the CVD method

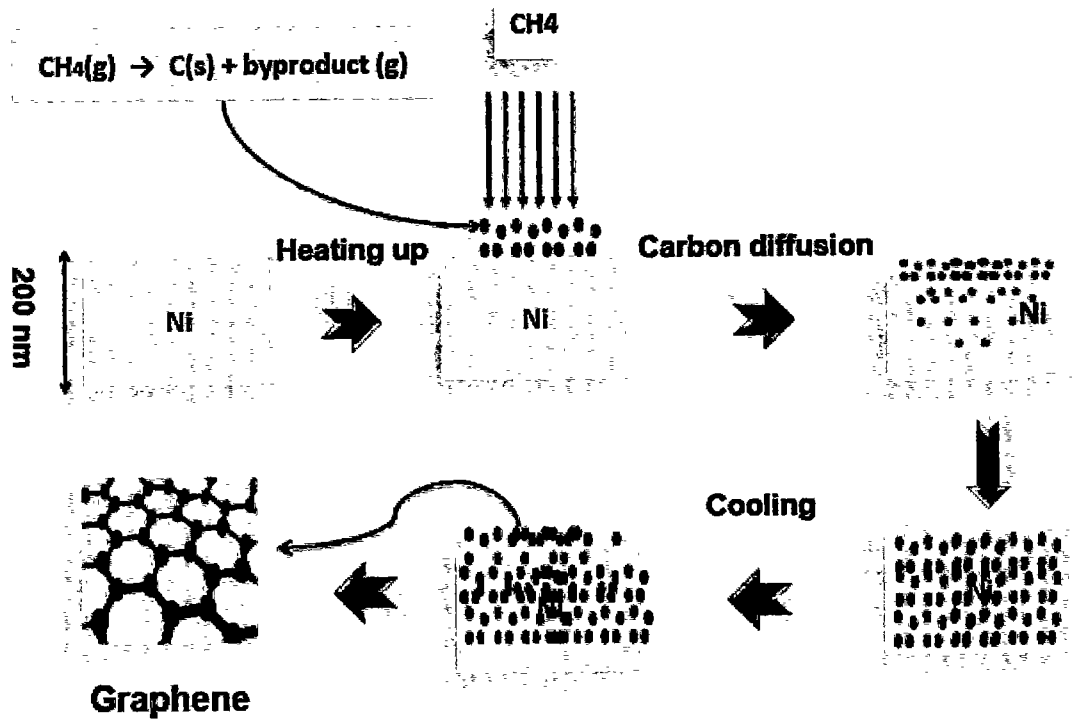


Figure 2.5: General scheme for CVD graphene growth on Ni substrate

First of all, a metal substrate for example Ni is heated either by a furnace or some other constant heating source up to 1000 °C under lowest vacuum pressure [25]. Methane and hydrogen gases are passes through the chamber in which the plasma state is already crated. The hydrogen acts as a catalyst to crack the methane bonds and after cracking when it hits the heated metal substrate its starts diffusing. After sometimes finally the supersaturation in

which the corban atoms segregated on the surface of Ni to form graphene layers. Here the main factors which mostly effect the CVD processes for graphene production is the numbers of graphene layers which you want to grow, temperature of the target substrate, cooling rate, type of the target metal substrate, thickness of the substrate and the solubility of carbon atoms into the target substrate. For example, for single layer of graphene one will prefer Cu as substrate because the solubility of Corban in Cu is less than Ni which will be used to grow multi layers of graphene.

Chapter 3: Graphene Literature Review

In this chapter we are presenting a review on some important topics related to our research like the CVD process for graphene growth on transition metals and specially on Ni substrate, next we will discuss that why we are using some specific dimensions of structure, graphene and metal interface, contact materials and graphene transistor modeling. Graphene is very sensitive material and all the properties of graphene totally depend upon how we are going to deal with it. In dealing with graphene the first step is by what method the graphene is synthesized because the quality of graphene should be high and there should be no contamination because any contamination even though only single atom of other material may affect the properties of graphene so all the requirements for synthesis of graphene should be fulfilled. Next as we discussed earlier that graphene is very sensitive material because all the properties of graphene changes when it becomes in interface with other material so it's very difficult to tackle because the graphene thickness is in nanometers so in this chapter we also discussing some work done with graphene metal interface and all its effect on the graphene properties and the combine properties of interfaced structures.

3.1 CVD Graphene a Review:

Graphene a 2D form of carbon having a honeycomb structure drawn attention of many scientists due to its unique electrical, mechanical and optical properties. Due to the

importance of this wonder material many research and review papers has been published. These papers present the general perspective of graphene research like graphene electronic properties, graphene based photonics and optoelectronics, graphene synthesis, graphene transistors and graphene application in energy storage as well as bio sensing application. Many journal has been reported on the chemical vapor deposition growth of graphene on metal surface. CVD method for graphene was first time reported in 2008 and with time to time it has been modified due to some important factors like cost, graphene quality and throughput of the system.

The basics of general CVD methods are discussed in chapter no 2. Here we will discuss application specific CVD in which the target metal substrate will be Ni.

3.2 Graphene synthesis on Ni:

Y. Zhang et al, explains in their review journal the most promising and widely used CVD method for graphene growth on Ni substrate [26]. We are explaining this method in very detail as the matrix we are using in our research is grown on such technique.

Generally, at the starting point the polycrystalline Ni is annealed in the presence of Ar/H_2 up to 1,000°C at atmospheric pressure. The annealing is done to increase the grain size and to minimize impurities. The annealed Ni substrate is exposed to a mixture of hydrogen and

methane gases. In this step the bonds of the methane break and the carbon atoms starts to defuse inside the heated Ni substrate as shown in Figure 3.1 and form a solid solution. At the final stage of the CVD process the sample is cool down in the presence of Ar gas. At high temperature like 1,000°C compare to Cu, Ni has the highest carbon solubility and gradually decrease with decrease in temperature [27].

During the cooling down process the segregation of carbon atoms occurs which means that carbon atoms diffuse out towards the Ni surface to form graphene layers.

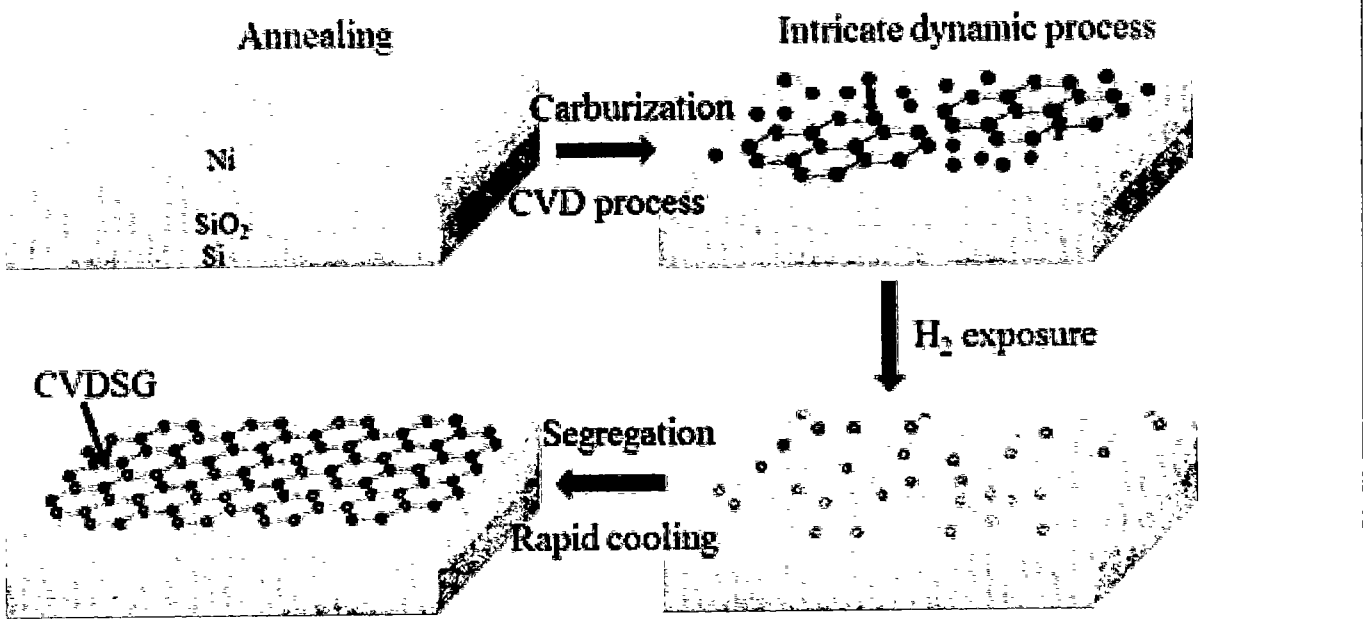


Figure 3.1: CVD method for Graphene growth step by step [28]

Ni is used mostly for graphene growth because Ni and graphene have relatively similar hexagonal lattice and similar lattice constant [29]. To grow single layer of graphene the

preferable metal substrate is Cu, because the solubility of carbon is less than as compare to Ni and for bilayer and beyond Ni is the best choice.

The growth of graphene on Ni substrate by CVD is a combination of two sub processes in which no 1 is the precipitation and the 2nd is the carbon segregation process. The segregation behavior is totally dependent on the cooling rates which directly effects the graphene thickness and the quality as well [30]. By medium cooling we can easily get few layers of graphene. Next the most important role in the graphene morphology is the structure and grain size in the Ni substrate.

T.H. Bointon et al, synthesized graphene by a new method known as a cold-wall chemical vapor deposition. They explained that this modified version of CVD is the most cost effective 99% cheaper than ordinary hot wall CVD and it is 100 times faster method for growing high quality graphene. Graphene produced through method has lowest defect density as observed by Raman Spectroscopy and the electron mobility's of 3300 cm^2/V. S measured through atomic force Microscopy also the quantum hall effect can be observed on single layer of graphene grown by this technique [31].

X.Chen, L. Zhang worked on the large area graphene grown by CVD. The main objective is to provide a detailed and recent review on the large area synthesis of graphene single, bilayer and multiple layers sing different substrate and upon the challenges in the production of

graphene. They used many target substrates like Cu, Ni, Pt, Ge, Ir, Co, Cu-Ni alloys which shows different growth manners in terms of single and multiple layers [32].

L.Huang, Q.H. Chang et al, reports the synthesis of high quality graphene on Ni substrate using a cold wall reactor by Rapid thermal chemical vapor deposition. In this new emerging method, they skip the step of carbon precipitation mechanism and used a shortest time of 10 seconds for production of graphene films. There results show that the graphene grows in the absence of hydrogen precursor has the lowest sheet resistance of 367 ohm/sq and the optical transmittance of 97.3% for 550 nm wavelength which is much better than graphene grown by ordinary hot wall CVD method.

The data suggests that graphene grown on this method have comparable electrical and optical properties to those grown by CVD on Cu substrates [33].

They also find the graphene grown on such technique can be directly transferred to any target substrate without casting a PMMA to minimize the chance of any contamination and impurity.

3.3 Graphene transistor matrix:

The structure we are using in our research work is known as graphene transistor matrix. The growing technique is chemical vapor deposition in which graphene is directly deposited

on $Ni/SiO_2/Si$. Ni is used as catalyst to grow graphene on its surface. The thickness of graphene surface is not uniform it vary from 1 to 10 layer due to the specific thickness of Ni. The average is taken to be 4 layers with thickness of 1.23 nm measured by spectroscopic ellipsometer available in advance electronics lab at IIUI. The specification of the transistor matrix is listed below

- Wafer Size: 100 mm in diameter
- Growth Method: Chemical Vapor Deposition Technique
- Film thickness: 1-10 monolayer
- Average layers & thickness: 4 layers, 1.23 nm
- Graphene film is multilayer with thickness varying in the range 1-10 layers;
- Nickel film is deposited on the substrate covered by thermally grown oxide layer
- Ni layer thickness is 400 nm;
- silicon oxide layer thickness is 500 nm;
- The thickness of the wafer is 500 μm;
- The crystallographic orientation of Si is 100 (Miller indexes);
- Defect density of films is very low;

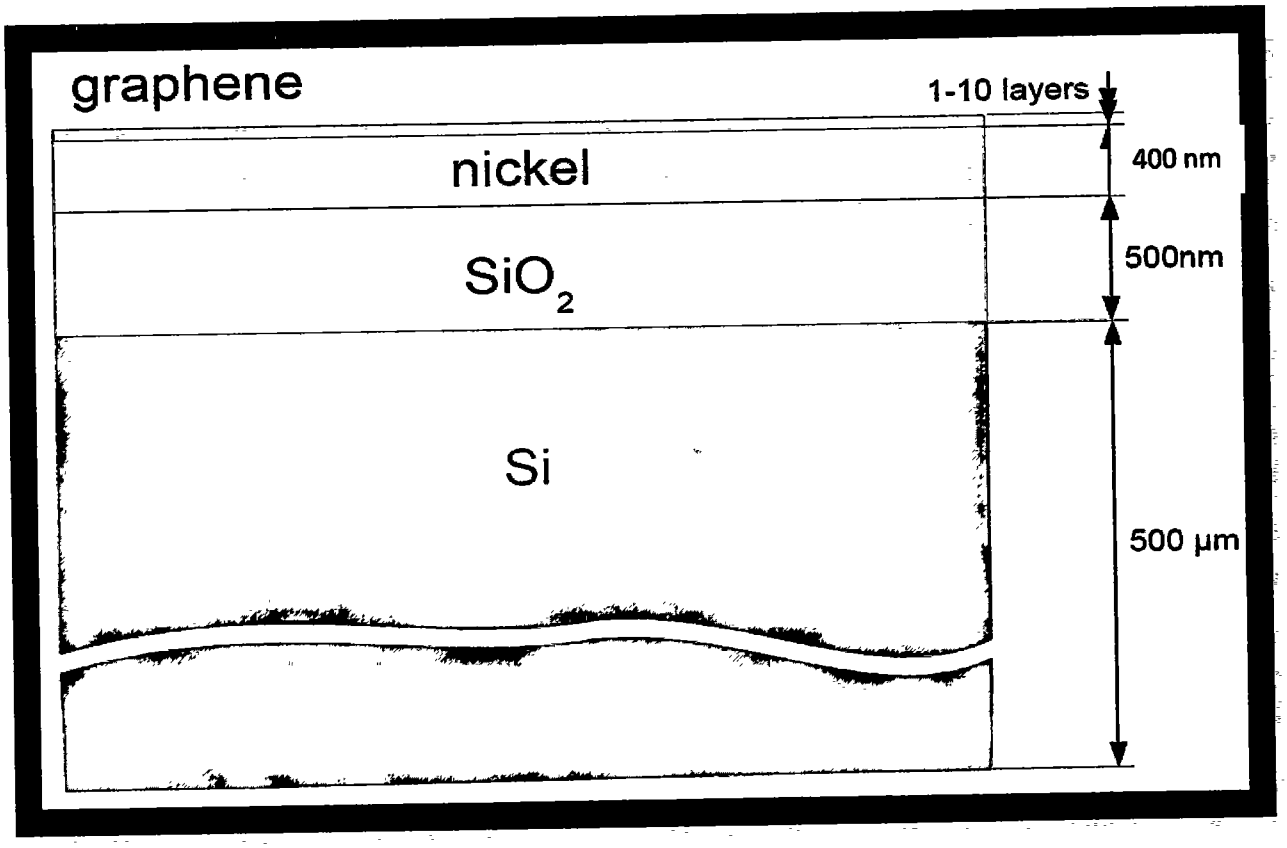


Figure 3.2: graphene transistor matrix specification

3.4 Graphene metal interface:

As we study in chapter 2 that intrinsic graphene sometimes called the suspended graphene possess some extra-ordinary properties like the ballistic transport of charge carriers with the speed of light having no mass, highest electron mobility's, excellent conductor of heat and energy, optical transmittance of 97.3% and the young modulus of 0.5 TPa [34]. The most important property of graphene is that it's neither a metal neither semiconductor because the electron of graphene can only be characterized by Dirac cones which have the relativistic properties like light. There are some other related sub properties to the above mentioned in

which the first one is the lowest sheet resistance due to its 2D nature of graphene, the 2nd one is lower resistivity, the 3rd one is highest conductivity, the 4th one is carrier concentration and the 5th one is the mobility of graphene. Now the properties we discussed are directly affected when we make an interface of graphene with metals, semiconductors and insulators or graphene is sand witched between other two materials may be between two metals or metal and semiconductor or metal and an insulator. This due to a fact that the fermi level of graphene changes when interfaced with another material which have different work function than graphene either the work function of the other material is less or greater than graphene due to which the fermi level of graphene changes this phenomenon is called the fermi level pinning. Here we are presenting a review on the previous work done on the graphene and metal interface.

C.Gong et al, investigated the first principal study of graphene and metal interface. They used 12 interface metal and study the electronic behavior of the interface structure, graphene doping types with the fermi level pinning and the doping density profile. They divided the interfaces in to physisorption and chemisorption. The metals like (Ag, Pt, Al, Au, Ir) forms a physisorption interface while the metals (Ti, Ni, Ru, Co, Pb) makes a chemisorption interface with graphene and concluded that for practical application the key parameter is the external

applied electric field which can be used to modulate the fermi levels and also to control the doping levels profiles [35].

Z. Xu et al, worked on the mechanical interaction of graphene and metal interface and focus on two the most important metal substrate Ni and Cu, because both of these metals used as a catalyst to grow graphene by the chemical vapor deposition process. The target is to find the mechanical interface cohesive energy, atomic geometry and strength. In their result they find out that due to same geometry and same lattice structure the interface between graphene and Ni has the highest cohesive energies than that of Cu interface with graphene. The results they found are totally based on density function theory [36].

3.5 Contact metals for graphene devices:

As we know that intrinsic graphene has the highest electron mobility but when it becomes with contact its mobility degrades because the contact resistivity is the performance killer for graphene devices. The important thing is which kind of contact graphene form with different transition metals. Studies and experimental work suggests that many metal/graphene contacts are ohmic in nature due no band gap relatively similar to metals. The values of metal/graphene contact resistivity are very high due to some limitation, in terms of physics called the (DOS) density of states means that the density of states in graphene is very less causes the high contact resistivity. In this section of thesis, we are going

to discuss issues related to metal/graphene interface effects on contact resistivity and the methods to reduce the contact resistance, also the techniques to find the contact resistance.

3.5.1 Carrier injection:

The tunneling current which enters from metal to graphene, if we look at it by the view point of electrical transport which is directly proportional to the density of states and so to the transmission probability. We know that density of states of metal/graphene has inverse relation with the contact resistivity [37]. Also by considering the term transmission probability, the important factor included is the momentum of charge of the charge carriers and the separation distance between metal and graphene. Now it is totally dependent upon the metal whose charge carrier's matches with that of graphene charge carriers. Another important factor is the fermi wave number, larger the fermi wave number so the larger is the fermi wave sphere and it will make the separation distance increase. For example, the Al and graphene have high contact resistivity due to the oxidation of Al in open air and can be used as top gate insulator.

The grain size of the deposited metal on graphene surface creates fluctuations and causes to increase the contact resistivity [38]. Also to create density of states in graphene by chemical doping or by ion implantation, it is not an easy task because the C-C bond is very strong so it will need a lot of energy to break the bonds. Theory suggests that the metal/graphene

interface can be divided into two groups one is physisorption and the other is a chemisorption group. These groups are already briefly discussed in the previous section. The method to calculate the density of states in graphene includes the scanning tunneling microscopy, photo-emission spectroscopy and the C-V analysis.

3.5.2 Energy band diagrams:

As we know that a metal and semiconductor form a schottky contacts while the metal/metal contacts are ohmic in nature. Now in the case of graphene the metal/graphene the situation is quite similar to that of metal/metal ohmic contacts because the graphene is a semi-metal with zero bandgap. The bandgap engineering in metal/semiconductor, metal/metal, and metal/graphene are shown in Figure 3.3:

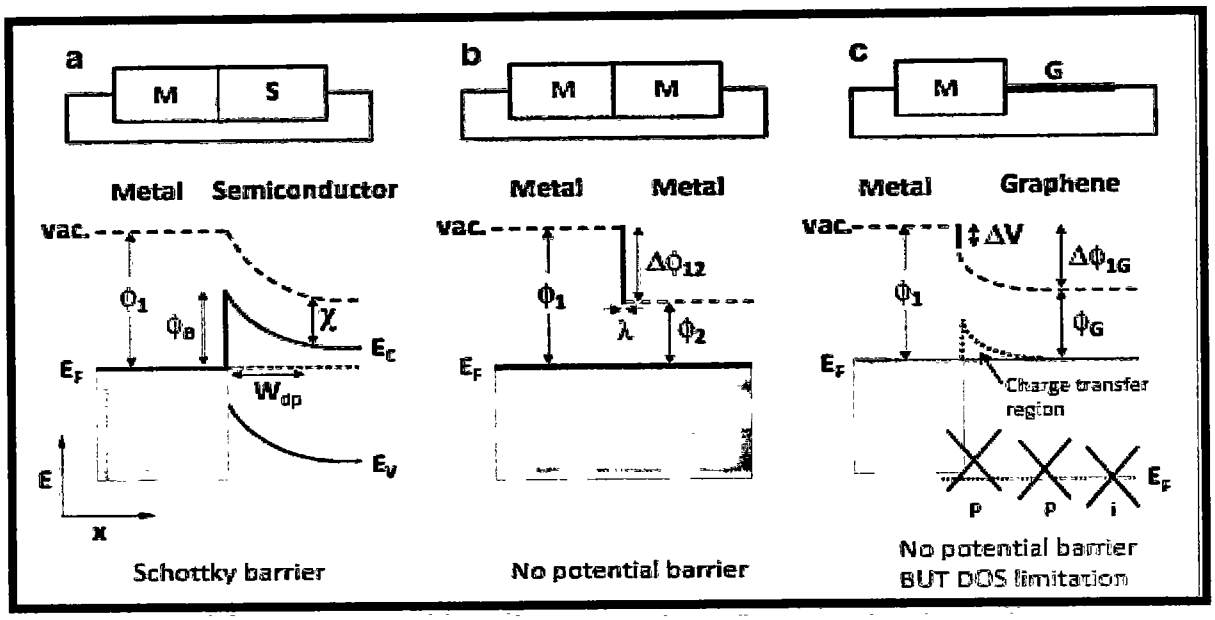


Figure 3.3: energy band diagram for (a) metal/semiconductor (b) metal/metal (c) metal/graphene contacts.

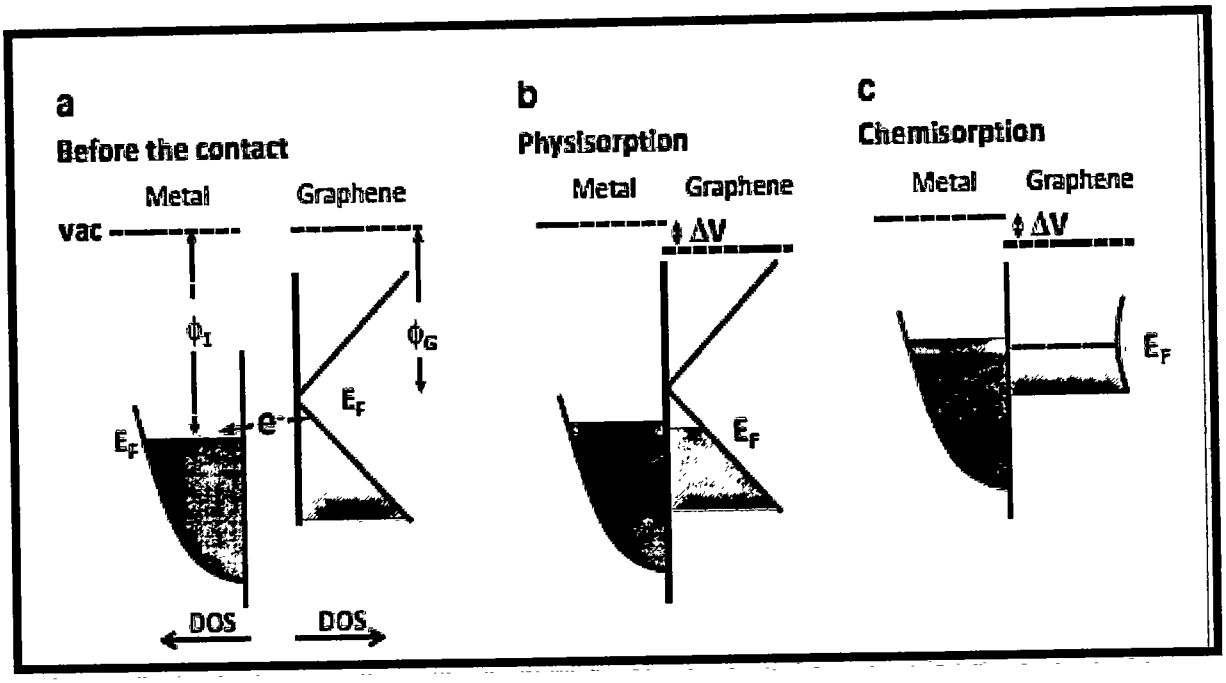


Figure 3.4: The relation between the density of states and the energy at the metal/graphene interface (a) before and after the contact formation (b) physisorption metal (c) chemisorption metal [39]

Figure 3.2 and Figure 3.3 shows the complete process in terms of energy band diagrams that's how charges can transfer from metal to graphene surface in case of chemisorption and physisorption contacts. The finding shows that the graphene work function is 4.5 eV [40]. Now what is the practical methodology to find the contact resistivity of metal/graphene interface? The most reliable method for this purpose is the (TLM) transfer length method which will be explained in the next chapter based on the characterization techniques.

3.6 Graphene Field Effect Transistor:

As we know that generally an FET (Field Effect Transistor) is composed of 3 electrodes known as source, gate and drain and during the conduction mode the majority and minority carriers are actually dependent upon the doping types of the substrate. For example, in n-MOSFETs the electron are the minority carriers due to the p-type doped substrate. Similarly, a dual-gate FET has four has four electrodes and it has advantage over ordinary single gate FET in terms of high switching rates, low power consumption and minimum noise. The 3 electrodes in FET are equivalent to emitter, base, and collector in BJT. Recently there are different types of FETs has been developed for the requirements of modern technology application, some of them are silicon, carbon nanotube, organic field effect transistors and so on. But some of them are not actually fulfilling the requirements for current and future technology application in terms operating frequency, miniaturization in size, noise, leakage currents etc. According to Moore's law the no of transistors in densely packed are should become double every two years, so to fulfill the prophecy of Moore's law we should have to miniaturize the size of transistor every two years. But now we are at the stage that further miniaturization of these devices and materials from which they are fabricated are not thermodynamically stable at room temperatures so we have to rely on some other emerging materials which would be thermodynamically stable in this critical situation and can be

further miniaturized to keep going on the Moore's law. This leads us to a new era of two dimension materials and the most promising is the Graphene. As discussed in the early topics the complete details about graphene that why it is so important to use graphene due to its some extraordinary properties

3.6.1 Graphene-FETs:

Graphene has the highest electron mobility and quite unique band structure which makes it a suitable candidate to be used for field effect transistor applications. To overcome the encountered obstacle in carbon nanotubes, silicon nanowires and organic materials graphene can be used as a channel material in the field effect transistors. The most important thing about graphene FETs that it can follow Moore's law and can further be miniaturized.

3.6.2 Field Effect in Graphene:

Graphene a semi metal with zero band gap and the charge carriers according to fermi Dirac statistics having no mass and can be converted from holes to electron and from electron to holes by applying an electric potential also at the Dirac point the electric field as well as the concentration of charge carriers becomes zero [41]. Positive voltage at gate input graphene becomes and electron conductor while negative voltage at gate input graphene conducts holes as a majority carrier. From quantum hall effect theory, in an experiment from

conductivity and hall coefficient we conclude that gate voltage is responsible for converting the charge carriers from holes to electron and vice versa.

3.7 Graphene FETs Structures:

The highest electron mobility and unique band structure makes graphene a promising material for transistor application like FETs. Here we are discussing different structures of graphene based field effect transistors.

3.7.1 Back-gated GFETs:

In this model the CVD graphene is transferred to a dielectric substrate or directly grown on the dielectric surface by roll to roll method. A lithographic and reactive ion etching are performed to make metal electrodes on surface of graphene. The first graphene channel based back-gated field effect transistor was fabricated by the graphene inventor K. Novoselove and his team in 2004 as shown in Figure 3.5:

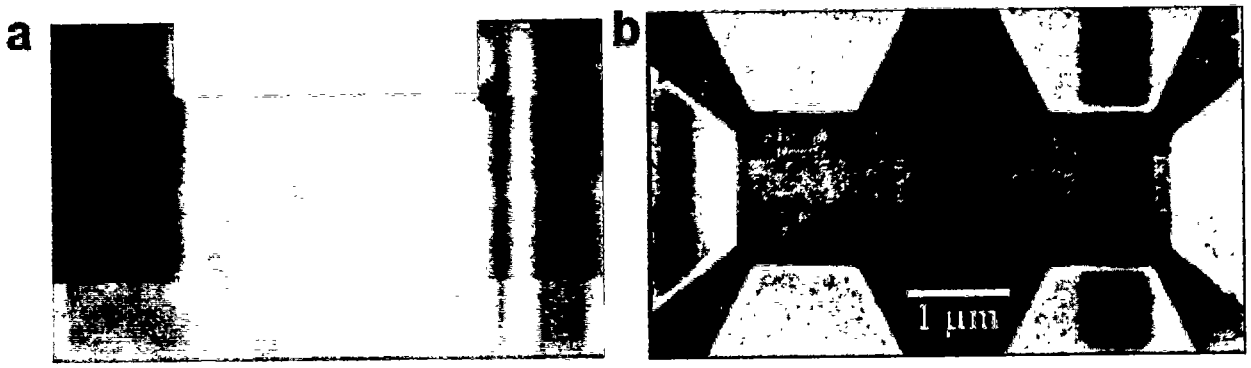


Figure 3.5: (a) schematic diagram (b) SEM image of back-gated FET [42]

In the above image the slight darker part is graphene channel while the darker part the dielectric layer of silicon dioxide.

3.7.2 Graphene top-gated FETs:

Here in this model a CVD grown graphene film is used as a channel material while silicon dioxide or PMMA is used as a gate dielectric as shown in Figure 3.5.

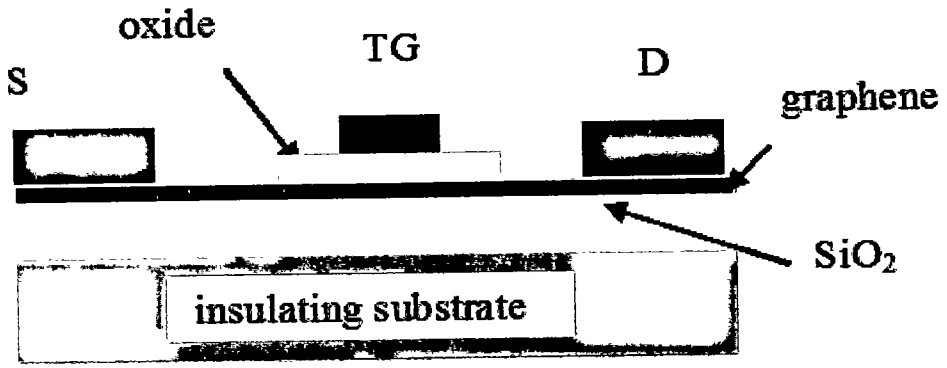


Figure 3.6: schematic diagram of graphene top-gated FET [42]

The metal gate is fabricated on the surface of dielectric. In circuit application point of view, the top-gated GFETs are more flexible than back-gated GFETs but the carrier's mobility is lower than back-gated GFETs. The reason is that the gate insulator scatters the charge carriers. Another dis-advantage of top-gated GFETs is that during the fabrication of top gate the chances for graphene damage increases throughout the processes. So here we conclude that getting high carrier's mobility using a top-gated graphene FET is very crucial and need very fine processing steps to fabricate it.

3.7.3 Dual-gated GFETs:

Here we are using two gates one top and another back gate. The highly doped silicon is used as a back gate while the metal electrode is used as a top gate as shown in Figure 3.6.

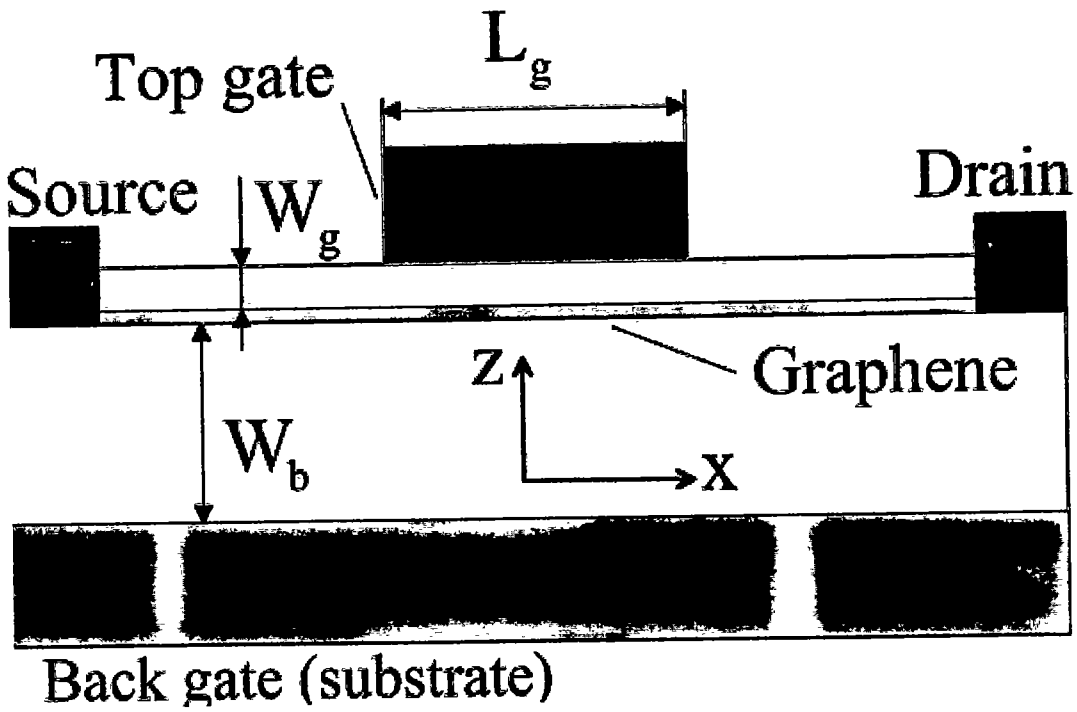


Figure: 3.7: Schematic of dual-gated graphene field effect transistor [43]

The model shown above is designed to study the I-V characteristics of graphene channel. Poisson equations are used to evaluate the top and back gate voltage parameters. The theoretical and experimental work combine shows that the top gate voltage remain low, no matter how much you increase the current across the source-drain.

Chapter 4: Characterization Techniques, Material & Equipment's

4.1 Electrical characterization:

There are basically three stages of evolution in electrical characterization of materials. In the 1800s the conductance G and the electrical resistance R were considering to the physical quantities to characterize any material under consideration. Both R&G were obtained from the I-V curve. But later on experiments showed that resistance R is not uniform for different shapes and geometries of same material, which means that different the geometry different the resistance value. To solve this, issue the concept of electrical resistivity (2^{nd} level) comes to existence and it was proved that electrical resistivity or electrical conductivity is inherent property of intrinsic material and it is independent of the shape and geometry of the substance. This concept first times allowed scientists in history to experimentally classify the current carrying capacities of different materials.

Next in first decade of the 1900s scientists realize that resistivity is not the only fundamental parameter to electrically characterize any material [44]. The is due to the reason that there exist many material having different shapes and different geometrical structures but yet they have same electrical resistivity values, also many same materials may give different electrical resistivity values due to different techniques upon which they are synthesized which is a special case for semiconductors due to non-uniform doping profile. So it is clear in case of semiconductor only electrical resistivity is not enough for electrical characterization. So to overcome this issue quantum mechanical theories plays an important role and leads us to a 3^{rd} level to use some new parameters like the electron mobility μ and the carrier concentration to characterize the semiconductor materials.

4.2 Hall Effect:

In 1879 Edwin Herbert Hall at john Hopkin University discovered the Hall Effect 18 year before the discovery of electron [45]. Behind the Hall Effect is the basic physical principle of Lorentz force which is composition of two forces, the electric and the magnetic force. When a magnetic force is applied at right angle to a current carrying wire/slab so a new force can be observed due to the combine effects of electric and magnetic force. This electromagnetic force is perpendicular to both these forces and known as a Lorentz force. The direction of Lorentz force may be in both normal so to find its direction the concept of right hand rule with be used. Mathematically we can write the Lorentz force as follows

$$F = -q\,(E + v \times B) \text{ .... (1)}$$

In the above equation $q = (1.602 \times 10^{-19}\ C)$ is elementary charge on electron, E is the electric field, V is the charge carrier velocity and B is the magnetic field strength. For an n-type semiconductor as shown in Figure: 4.1 below:

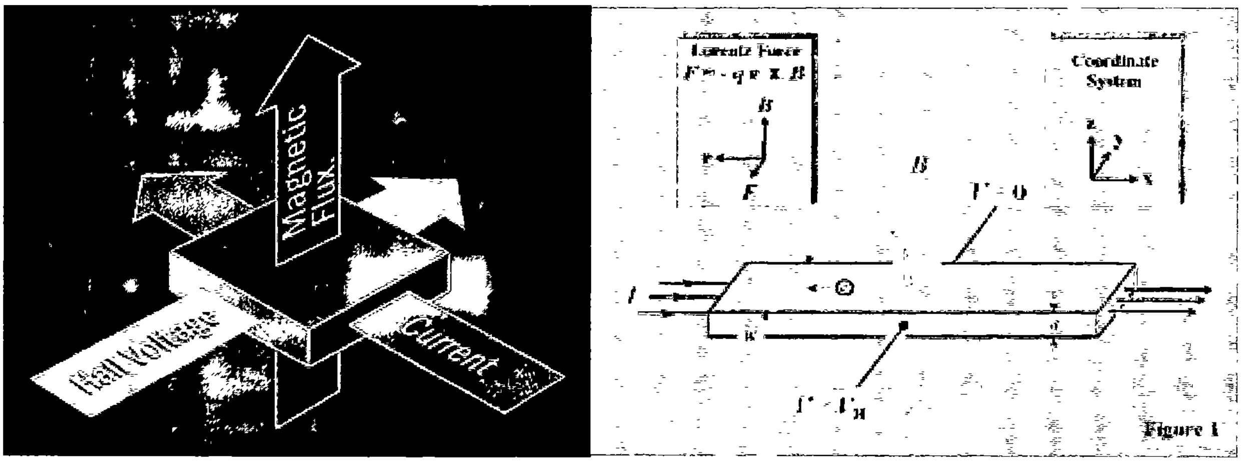


Figure 4.1: (a) basic schematic of Hall Effect (b) Hall Effect for n-type semiconductor (special case)

Let us assume that a uniform current flowing along the x-axis and the magnetic force is applied perpendicular along the z direction so the electron drift towards the y direction due to the Lorentz forces causing the excess of electron toward one side of the sample. This excess charges produce a voltage known as Hall Voltage is its magnitude is:

$$V_H = IB/\text{and} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(2)}$$

In equation 2 above d is sample thickness, B is magnetic field strength, q is charge on elementary particle, "n" is bulk density and I is the current. For a two dimension slab the term sheet density ($n_s = nd$) will be used instead of bulk density and equation no 2 in terms of sheet density can we written as follows:

$$n_s = IB/q|V_H| \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(3)}$$

to calculate sheet density n_s we have to first find the Hall voltage and then by knowing all other parameters B, I, q the sheet density can easily be found. The Hall voltage may be negative or positive it depends upon the type of semiconductor. Normally for n-type the Hall voltage is negative while for p-type semiconductor it observed to be positive. Conventionally the sheet resistance of a semiconductor can be found by the Van der pauw technique and will be discussed in the next topic.

To find the sheet resistance first we must know the values of sheet density as well as the electron mobility. The equation for mobility is:

$$\mu = |V_H|/R_sIB = 1/\,(qn_sR_s) \quad \ldots\ldots\ldots\ldots\ldots\ldots \text{(4)}$$

If thickness "d" of the slab is known so we can easily calculate the bulk density and resistivity as well.

4.3 The Van der Pauw method:

The Van der pauw method was first propounded by L.S. Van der pauw in 1958 [46] and commonly used to measure the Hall coefficient, resistivity and other properties of any 2D arbitrary shape sample. By this technique we can find the resistivity, doping type, carrier density and mobility of sample. Before using this technique there are some condition to be satisfied like the sample we are using for this technique should be perfectly flat with uniform thickness, next the sample should be isotropic and homogenous and contain no fracture defects or isolated holes, also the probe should be placed on the perimeter of the sample. Possible sample geometries are shown in fig 4.2 below

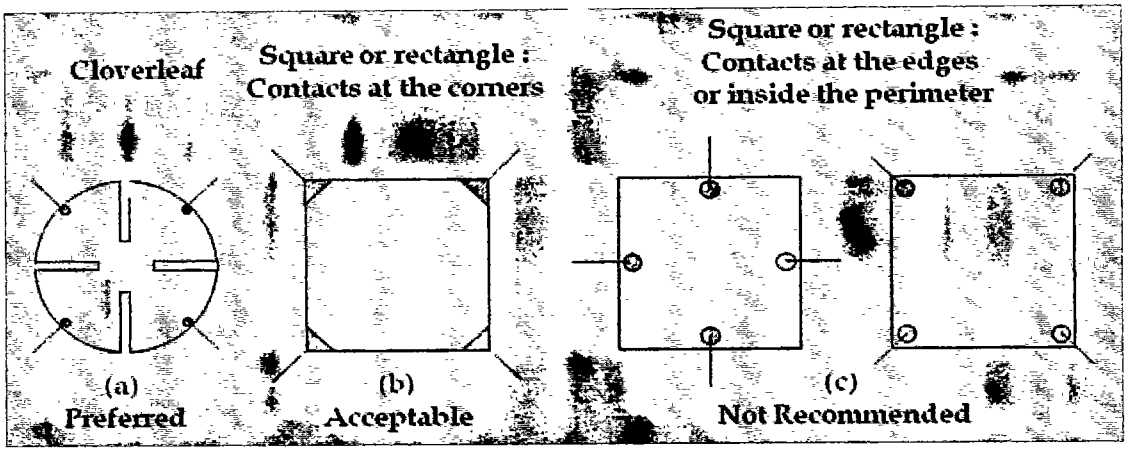


Fig 4.2: possible sample geometries for Van der pauw technique.

4.3.1 Methodology:

To find the mobility and sheet density the Hall measurements and resistivity measurements are needed. From resistivity measurements we calculate the sheet resistance Rs. In Van der pauw we have two types of characteristics resistances known as the R_A and R_B with respect to the terminals shown in fig 4.3 on the next page. Both the resistances R_A and R_B according to the van der pauw equation have the following relation with the sheet resistance.

$$\text{Exp}\,(-\pi R_A/R_S) + \exp\,(-\pi R_B/R_S) = 1 \quad \text{..... (5)}$$

and can be solved for sheet resistance as follows:

$$R_S = -\Pi/\ln\,(1/\exp\,(R_A) + \exp\,(R_B) \quad \text{..... (6)}$$

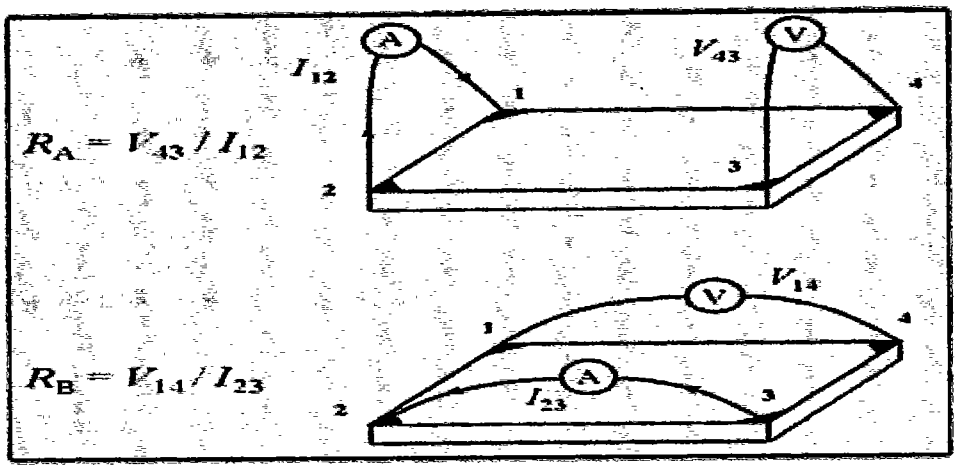


Figure 4.2(b): The Van der pauw terminal setup for finding R_A and R_B

The electrical resistivity of bulk can be calculated as:

$$\rho = R_S \times d \quad \text{..... (7)}$$

To practically calculate the characteristics resistances R_A and R_B a dc current is pass through contact 1 and 2 and the voltage is measured across contact 3 and 4, next the current is passes through contact 2 and 3 and the voltage is measured across 1 and 4 shown in Figure 4.2 above. R_A and R_B can be calculated as:

$$R_A = V_{43}/I_{12} \text{ and } R_B = V_{14}/I_{23} \quad \text{..... (8)}$$

By putting equation (8) in equation (6) we can find the sheet resistance R_S.

To find the sheet carrier density by using the van der pauw method we to need the Hall voltage so we have to perform the Hall effect measurements. In Hall Effect measurements we

have a constant magnetic field and a constants current while the voltage varies as the setup shown in Figure 4.3:

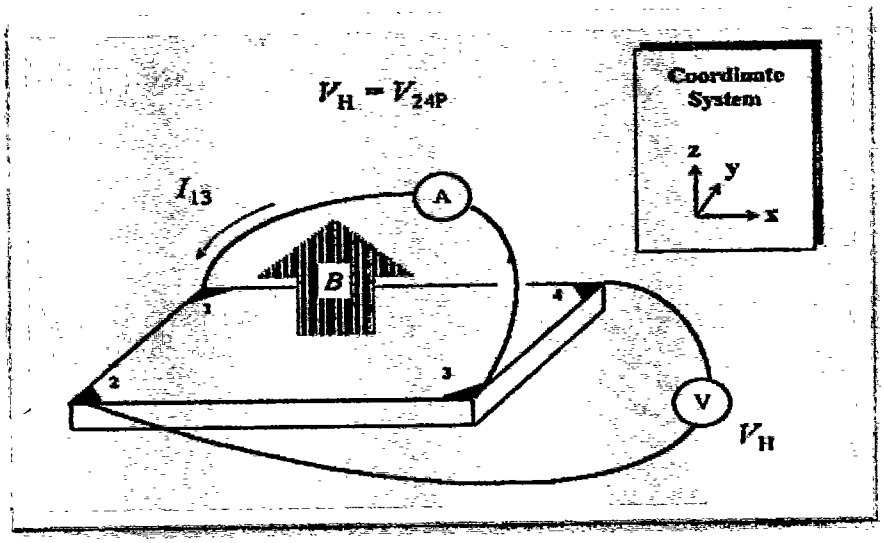


Figure 4.3: schematic of Hall measurements

As we see in Figure current is applied through contact 1 and 3 and the voltage V_H (= V_{24}) is measued and now by applying the formula of equation (3) we can get the sheet carrier density n_s.

There are some precautions for Hall measurements to be keep in mind.

(1) The contact must be ohmic and should be of precise size required for hall measurements.

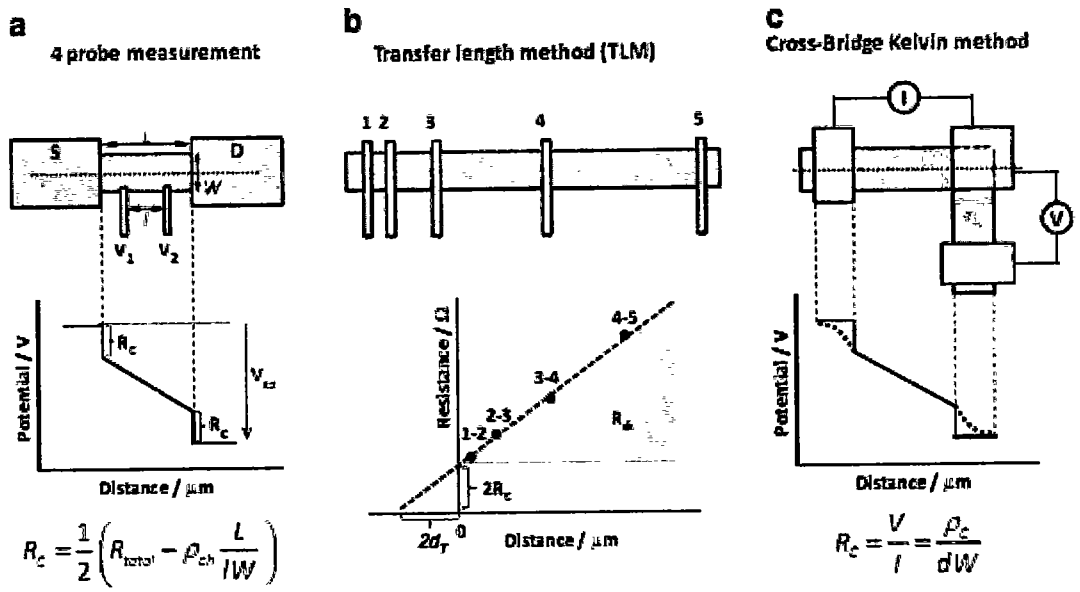
(2) The thickness of the sample uniform and also known

(3) During experiments the photoelectric effect must be minimum because some materials are sensitive to light so the experiments must be carried out in dark room

(4) Hall measurements needs uniform temperature because the non uniform temperature may create the thermomagnetic effect.

4.4 Transmission Line Measurements:

The transmission line method/transfer length method is a technique to find the value of contact resistance between metal/semicondutor junction. As we see in the Van der pauw method that 4 metal contacts were deposited on each corner of the sample to measure the sheet resistance and it was also mentioned that the contact should be ohmic in nature to minimize the contact resistance. But still there were contact resistance but we neglect it because it was consider to be minimum but in case of device performance like transitor application in modern technology it the major herdle in grpahene transistors. So in this section of the thesis we are going to discuss the methods to find the contact resistance of graphene and metal juntion by the new method of transfer length method. There are other methods too as shown in Figure 4.4, but the TLM is known to be an industrial standered so we will focus the TLM only.



$$R_c = \frac{1}{2}\left(R_{total} - \rho_{ch}\frac{L}{lW}\right)$$

$$R_c = \frac{V}{I} = \frac{\rho_c}{dW}$$

Figure 4.4: (a) Four-probe measurement, (b) transfer length technique (c) cross-bridge Kelvin technique [47]

4.4.1 Methodology of TLM:

Step1: junction preparation:

The first step is to deposite the metal contacts by mean of any technology like thermal evaporation and pattern them in form of metal pads separated by a distance apart as shown below:

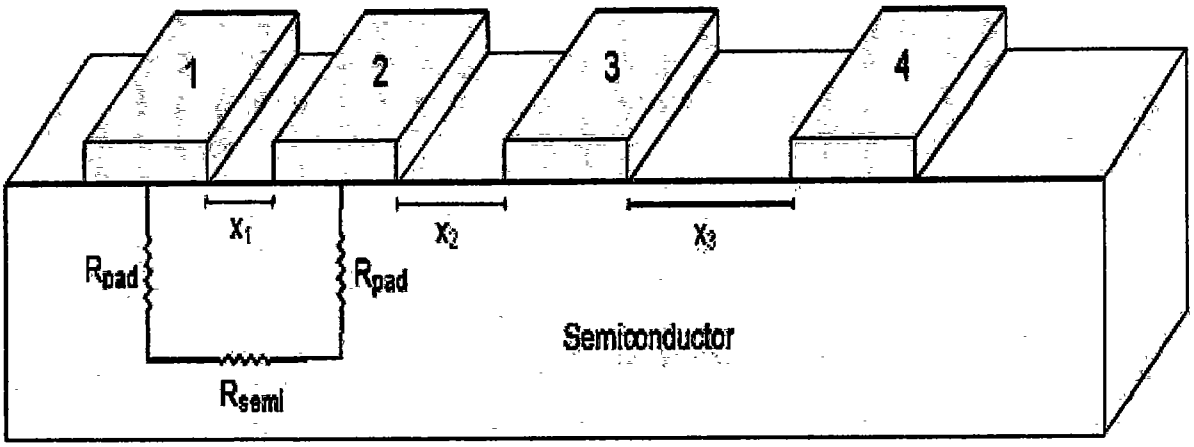


Figure 4.5: Metal pattern for TLM separeted by a varying distance

The size of the pade must be the same but the distance after each pad must vary. After the formation of metal pades the annealing must be done so the metal may diffuse to form a junction with semiconductor or in our case is the graphene.

Step 2: Measurements:

In this step we have take the simple I-V readings to calculate the resistance between each pad. The method is very simple it can easly be done at the probe station or some other parameter analyzer. Resistance should be found by simple R=V/I

Step 3. Contac resistance calculation:

As shown in Figure 4.6 the resistance between any two pads can be consider as three resister in series, one from metal to graphene/semiconductor, through the graphene, back to metal. Since as we mention before that the contact should be ohmic in nature so the polarity of the input voltage source produce no difference so the total resistance between each consective pads are:

$$R_t = 2R_{pad} + R_{graphene/semi.} \quad \text{..... (9)}$$

Now we have to plot the resistance of the two pads vs the distance they apart from each other we get a graph like this shown in Figure 4.6.

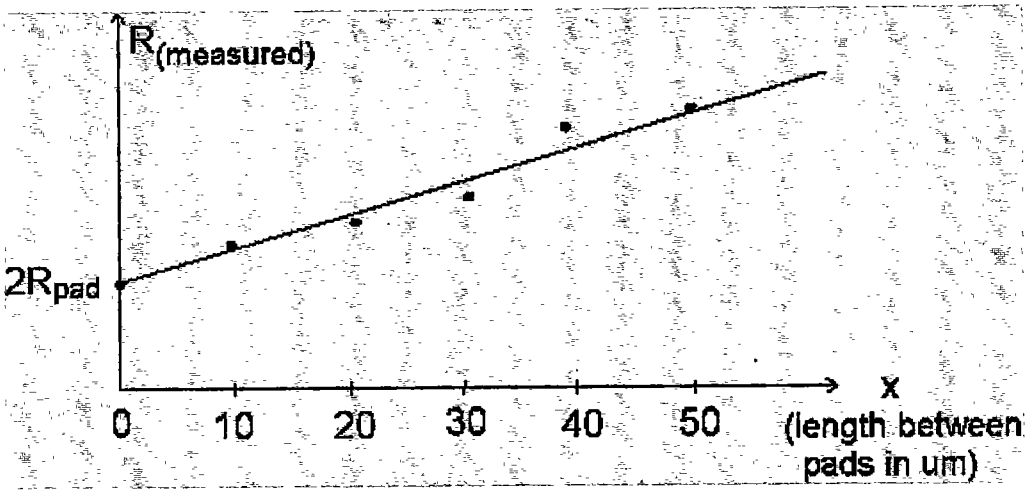


Figure 4.6: plot between resistance and separation of 2 pads.

If the two pads are so close to each other that the distace between them becomes zero so according to equation (9) we can write as

$$R_t = 2R_{pad} \quad \text{..... (10)}$$

From equation (10) we can easily find the contact resistance and by putting it in equation (9) we can calculate the resistivity of graphene/semiconductor.

4.5 Equipments:

In this section of the thesis we are going to discuss about the equipments which we are used throughout our research. Each indvisual is listed by name as below

(1) Nano-chip reliablity grade hall effct system

(2) Automatic system of materials electro-physical charaterization

(3) Thermal evaporator

(4) Rapid thermal annealer

All these equipments mentioned above are present in working condition at (AEL) Advance Electronics Lab Internation Islamic University funded by the Islamic Development Bank. Now we are going to discuss each equipments one by one in detail and the role ot each equipment in our research.

4.5.1 Nano-chip reliability grade Hall Effect System:

The basic principle behind the nano-chip reliabily grade Hall Effect system is the theory of Hall Effect system or we can say here we practically exercise the Hall Effect theorum. Hall Effect system is completely discussed in the previous section of this chapter with detail. Here we are discussing the practical application of Hall Effect system. The nano-chip reliabily grade Hall Effect system has the following units also shown in Figure 4.7:

Accusation unit	Sample Assembly
Permanent Magnet	Special grade axial wire
Liquid Nitrogen Chamber	Funnel

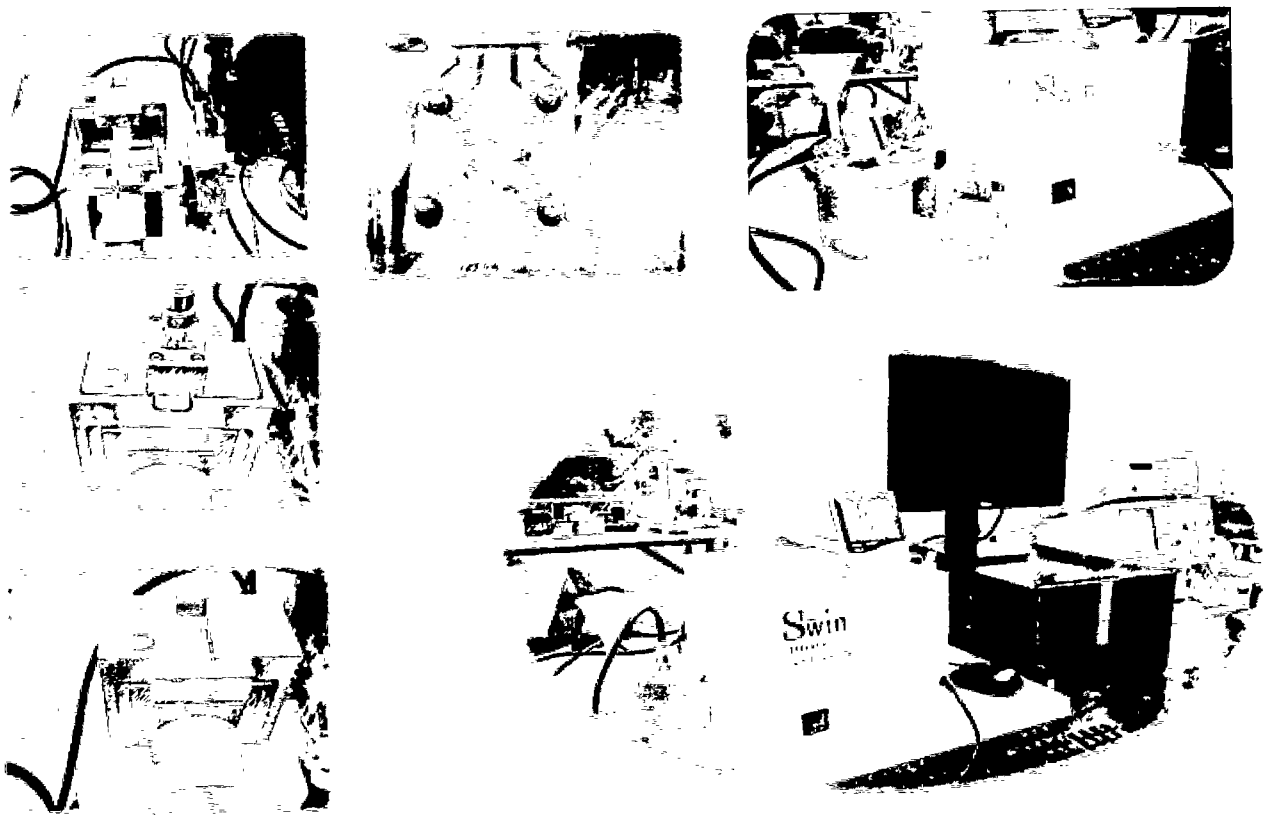


Figure 4.7: The basic units of nano chip reliability grade hall effect system. The image is taken by the authority permission of Advance Electronic Lab International Islamic University Islamabad.

The nano-chip reliabilty grade Hall Effect system is a device probing techniue and use the Van der pauw 4 point probing technique for sample preparation and characterization as explained before in details.

4.5.2 Application & Specification:

Application include a varity range of DC field measurements like wafer scale mobility as function of temperature and magnetic filed, cryogenic and high temperature ranges during measurements, data acquisition and system level analysis by intuitive built in software and supports exportation of data for Hall multi carrier analysis which include (sheet resistance,

electrical resistivity, electrical conductivity, Hall voltage and Hall Coefficient, nature of the conductivity, bulk concentration and mobility).

The system specification is shown in table 4.1:

Sample size	10mm x 10mm ~ 15mm x 15mm
Operating temperature ranges	Elevated, Ambient Room Temperature and cryogenic
Materials measurements range	Si, Ge, SiGe, SiC, GaAs, In GaAs, InP, GaN, ZnO, Graphene, Nano Particles etc.
Magnetic Flux Density	0.53 Tesla
Current Sensitivity	2 nA
Input Voltage ranges	1μV-300V
Carrier Density range	10^7 – 10^22 (cm-3)

Table 4.1: Nano chip reliability grade Hall Effect system specification

4.5.3Automatic System of Material Electro-Physical Characterization:

ASMEC is a tool for most advance level of characterization especially for ultra-low ampere resolution application. The application and specification and units of ASMEC is shown in the Figure 4.7 (a) and Figure 4.7 (b) on the next page. The images are added in this thesis by the permission of Advance Electronic Laboratory International Islamic University Islamabad. The ASMEC is in working condition and available for research and can be through proper channel as mentioned on University website.

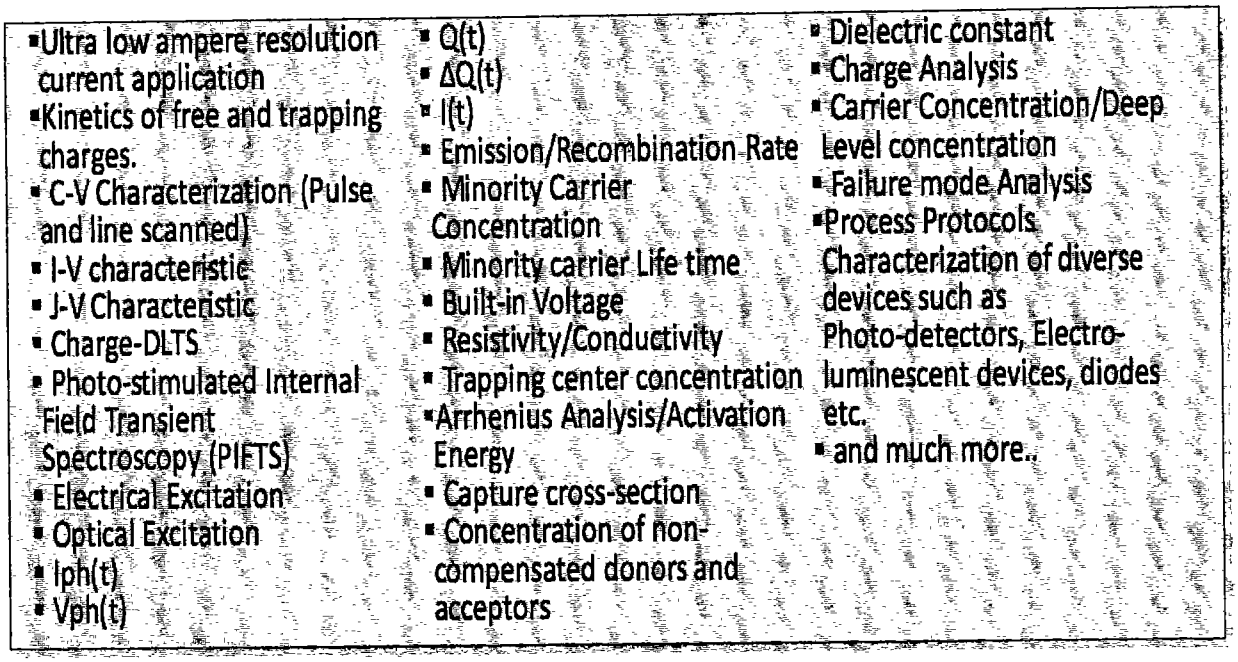


Figure 4.7: (a) ASMEC parameters and Application

The specification of ASMEC are shown in table 4.2 shown below

Current Sensitivity	• 1pA
Charge Sensitivity	• 5 E- 16C
Range of Bias Voltage	• -13.5V to +13.5V
Range of Rate window	• 10μs-200s
Temperature	• 72K-500K (Extendable)
Interface	• Probe-station /External Acquisition
Deep level concentration sensitivity	• 5 E -7

Table 4.2: ASMEC specification and operational ranges.

The main parts of ASMEC are listed below and also shown in fig 4.7 (b)

ASMEC Acquisition unit	ASMEC Power Supply.
JANIS cryogenic.	Vacuum cylinder
Flash light.	Lamp and heater

The acquisition unit contain a built in software based system to calculate real time parameters as shown in fig 4.7 (a). Cryogenic unit is used to maintain low temperatures in case of when readings are needed at 77K.

Figure 4.7: ASMEC main parts (Advance Electronic Lab) International Islamic University

4.5.4 Atomistic Layer Nano-master Deposition System:

For atomistic layer deposition and for interconnects formation we can use the Nano-master NTE system which is specially designed to achieve precise thickness without any contamination. The system uses a DC/RF source for sputtering process in which the metal pallets are placed in a crucible and a DC current is passed, due to high resistance of crucible the temperature rises and the metal starts to evaporate atom by atom and starts to deposit on target substrate. The system is controlled by computer with built in software to get high level precision and quality, the setup is shown in Fig 4.8 by the permission of AEL.

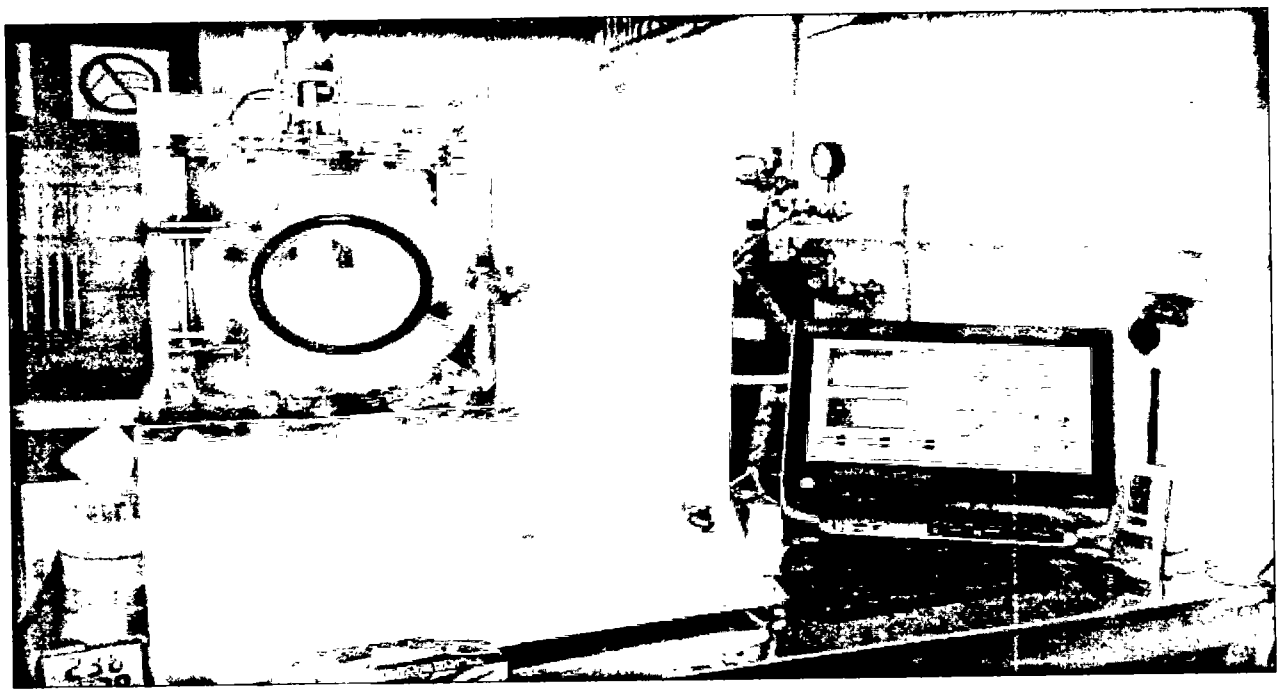


Figure 4.8: Atomistic Layer Nano-master Deposition System units.

Application include interconnects formation, connecting two components on a chip, packaging purpose, extremely thin film formation for solar cells and metal contacts for device and component electrical characterization.

4.5.5 Rapid Thermal Processing System:

Rapid thermal processing system is a computer base facility and can be programmed as per project requirements can supports temperature ranges up to 1500 °C. The processes for which the system can used include as an Annealer for metal contact in compound semiconductor, ion implantation and CVD like systems.

Rapid thermal processing system used in semiconductor industry for variety of application like in silicon micro-fabrication, Nano electro-mechanical system and also for photovoltaic application. The setup is shown in Figure 4.9 below.

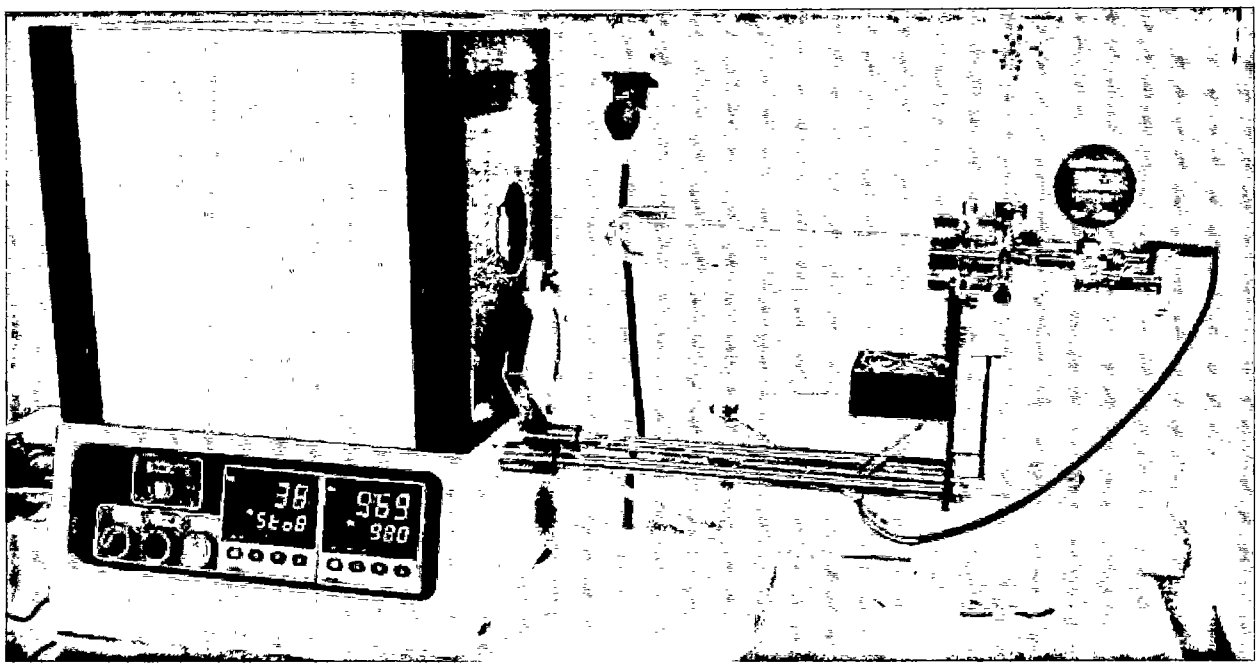


Figure 4.9: Rapid thermal processing system (Advance Electronic Lab IIU Islamabad)

In our research we are using the system as an Annealer after the contact formation because the contact resistance can be minimized by an applying a proper thermal flux.

Chapter 5: Samples preparation and experiments

This chapter is divided in to two sections no 1 is the wafer dicing and sample preparation and the section two is totally based on experiments which is further divided into two sub sections i.e. contactless measurements and contacted measurements. In section one of this chapter we are going to explain how we can dice a wafer by using a diamond cutter as we have used a diamond cutter in our case for dicing or cleaving the whole wafer. Next in section 1 we have to show how we can make samples for different tools as per the tools requirements like some tools may need a rectangular sample while some may need square samples like the Hall Effect system based on the Van der pauw needs a square sample for characterization.

In section 2 we are going to explain how we carried out the experiments on different samples prepared in section 1. In section 2 first we carried out contactless measurements using the Nano-chip reliability grade Hall Effect system to find out different parameters related to our sample. Next we have to deposit metal contacts as per system requirements to conduct contacted experiments on both the tools Hall Effect system as well as the ASMEC. For contact formation we have used the Nano master metal deposition system and for the annealing purpose the rapid thermal processing unit is used.

5.1 Wafer cleaving/dicing:

This is said to be a must have-skill for semiconductor engineers or researcher to cleave and dice a wafers and a need a perfect skill. There are a lot of methods used for wafer cleaving/dicing, some of them are conventional and some are industrial like diamond cutter is a conventional and cheap method while laser cutting is industrial fabrication standard and

is too expensive also. In our research project we are using a conventional method for wafer dicing/cleaving. For this type of cutting you will need a Si (100) wafer, wafer tweezer, diamond Scribe and a petri dish. First of all, we have to know the orientation then make scratch on the wafer side by diamond cutter. Next insert the tweezer tip beneath the cutting edge and gently push it from the side and the job in done as shown in Figure 5.1

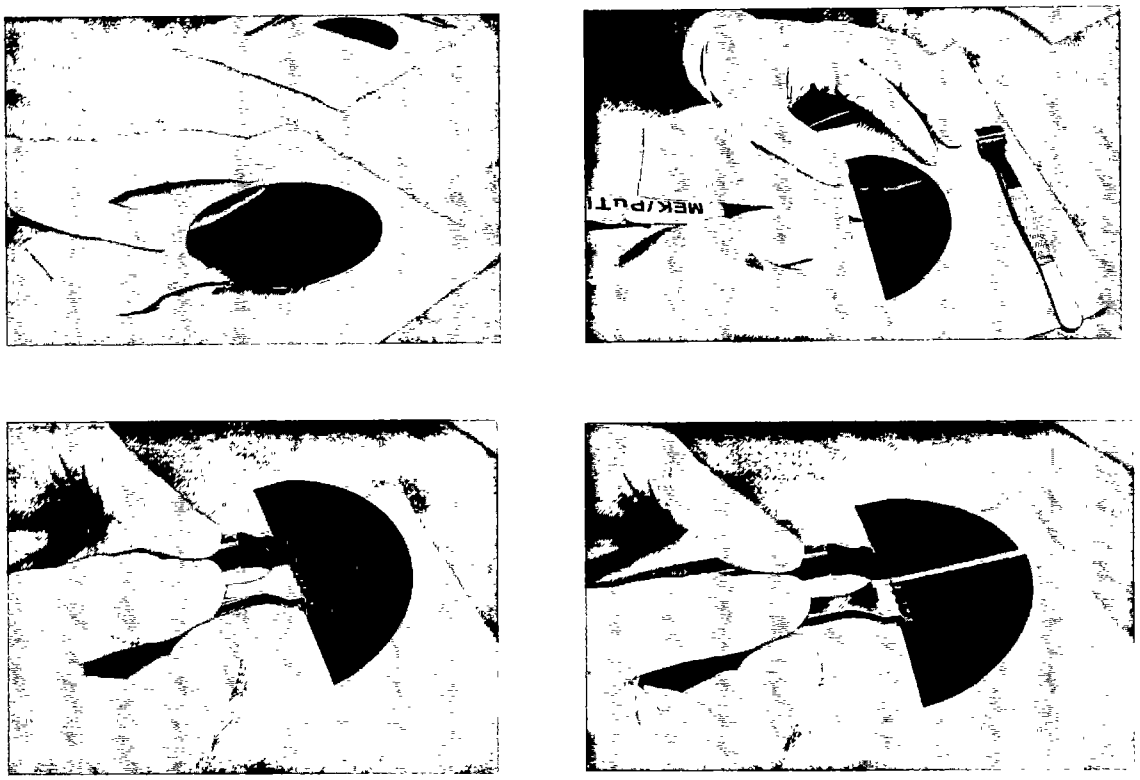


Figure 5.1: wafer cleaving in lab.

5.2 Sample preparation for van der pauw:

According to the basic requirements for the van der pauw method that the sample thickness must be less than the length and width of the sample also the sample must be symmetrical and contain no isolated holes. To get better result ohmic contact should be made by using a

deposition system and the contact should at the edges of the samples as we have made it shown in Figure 5.2 below.

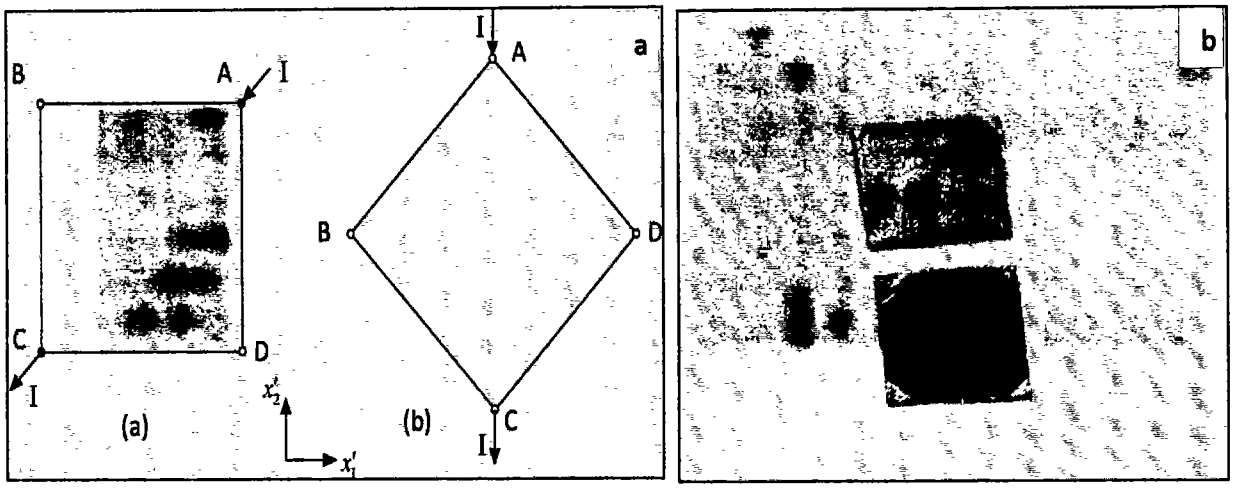


Figure 5.2: (a) possible contact placement (theoretical) (b) sample designed in lab

According to the van der pauw theory the metal contact should small as possible to minimize the effect of contact resistivity because the large surface area increases the contact resistance.

The most important thing to be keep in mind that all the contact we are going to made on the sample should made of same material because thermodynamically each material is different from other material and if we made contact of different materials it will create thermoelectric fluctuation and the result will not be reliable. We have used silver and copper as contact materials.

5.3 Transfer length model sample preparation:

Generally, the transfer length method is used to find specific contact resistivity between a metal and a semiconductor. Here we are going to show how we can design the samples for

transfer length method. First of all, a rectangular mask was designed with the dimension of 10×20 mm as per system requirements. The size of the metal pad is kept constant while the distance between each pad in row is kept variable. The metal pads are deposited by using the Atomistic Layer Nano-master Deposition System. The deposited metals are silver with the thickness of 50 nm means the thickness of each pad as shown in Figure 5.3 below.

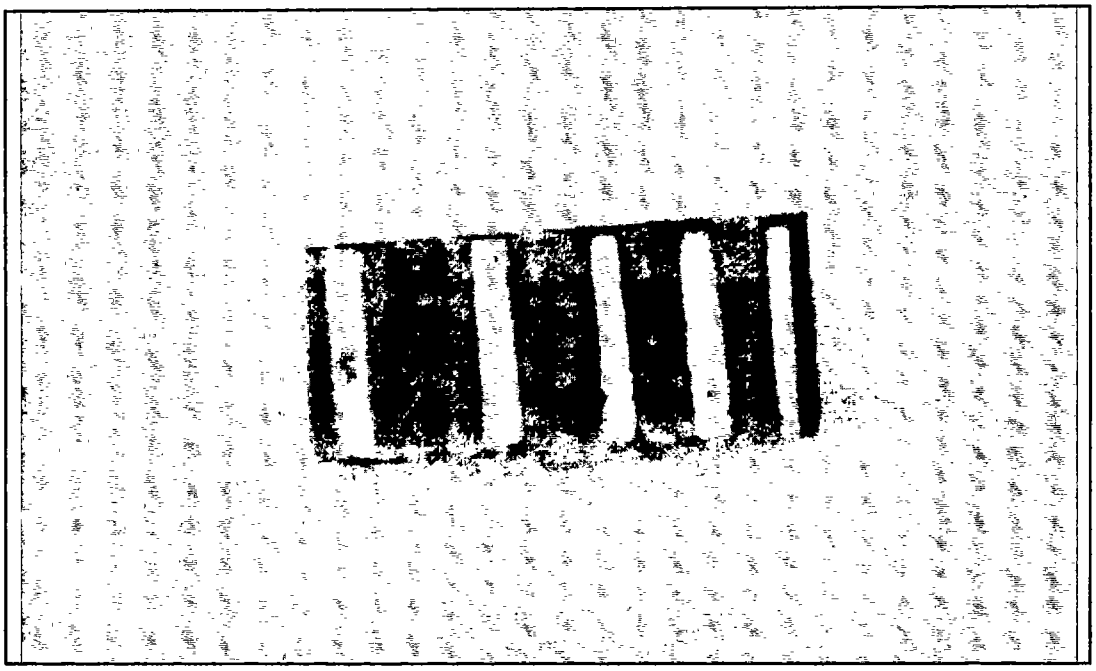


Figure 5.3: A TLM structure designed in AEL (Advance Electronic Lab).

The white color shows the deposited silver while the black color shows the graphene. Each pad has width and length ratio of 1×10 mm while the distance varies from 0.5 mm to 4 mm between adjacent pads from right to left as shown in Figure above.

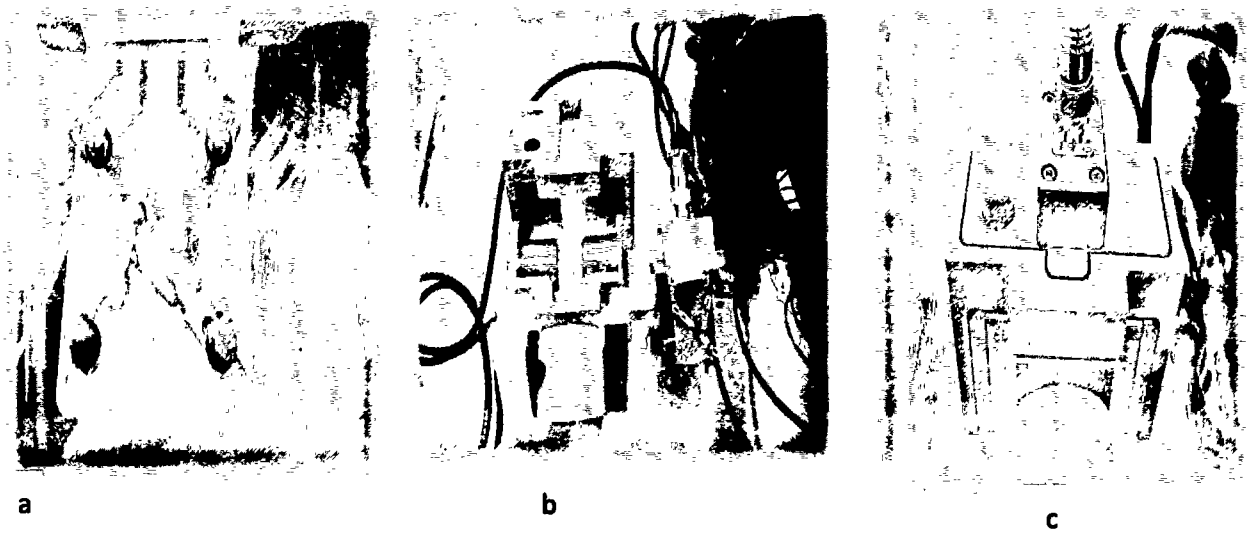
5.4 Experimental section:

In this section we are going to discuss the experimental work that we have done in lab. Actually the experimental work that we have perform is of two type the first one is a

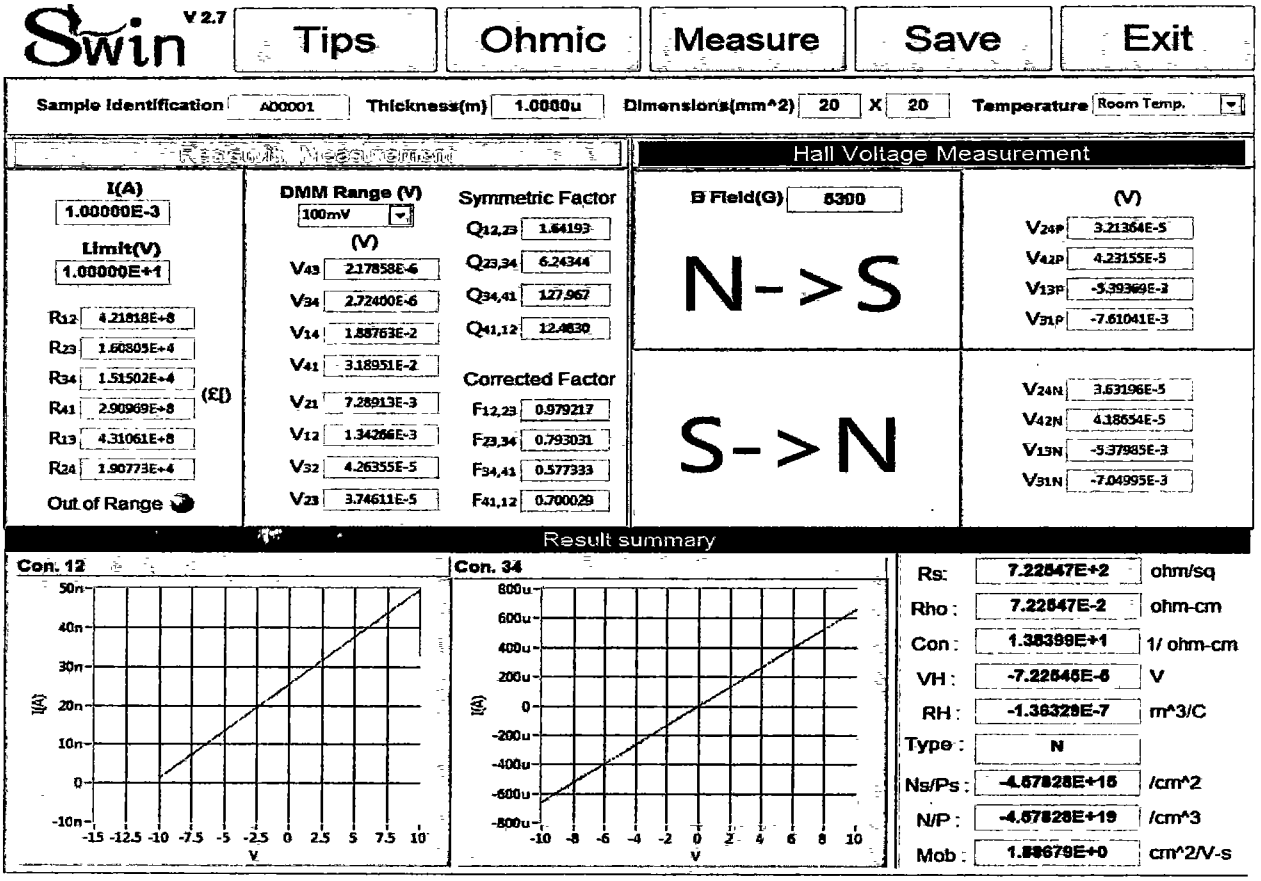
contactless or temporary contacts and the second one is the contacted work in which we deposit metal contact on target substrate. After the deposition the contact are annealed to make a perfect contact with the target substrate which is actually a CVD grown graphene on Ni surface also known as graphene transistor matrix. So now we are going to discuss the procedure of experiments and the steps involved in it one by one and the characterization method used in it.

5.4.1 Contactless measurements:

By contactless measurements we mean that the sample here we are going to use in our experiments does not contain any metal contact normally when we have to characterize a sample we need to deposit a target metal contact on its surface, but in our case we are going to compare the results before and after the contact formation. In contact less measurements the sample with a dimension of 10×10 mm is prepared by the cleaving the wafer. The sample is placed in a probe station by using a tweezer and the tips are placed on each four corner of the sample because we are using the van der pauw method for characterization. Here we are using the Nano-chip reliability grade Hall Effect system for the contactless measurements which is computer based system with a built in software to calculate and display the parameters related to the experiments. The sample is place inside a permanent magnet assembly line and starts the experiment. The setup is shown in the Figure 4.4 on the next page.



a b c



d

Fig 5.4: (a) sample placement (b) connecting wires (c) permanenet magnet (d) contact check and measurements

From Figure 5.4 we see the sample is placed for contact check either ohmic or schottky depends upon the substrate. After the contact check readings are taken and saved.

5.4.2 Contacted experiments:

Metal contacts are an obvious part of semiconductor devices and its reliability. The contact resistance should be minimum as much as possible for better performance of semiconductor devices. The metal-semiconductor contacts normally of two types ohmic and schottky contacts depends upon the metal and semiconductor interface. In our case we are considering the ohmic contacts because graphene is a semi-metal and the contact between metal-metal is ohmic in nature. Also in Figure 4.4 (d) during the Hall Effect for the contact check we get a linear I-V curve which indicate that the temporary contacts were ohmic in nature.

Also the deposited metal atomic level geometry has a vital role in the formation of ohmic contacts. For low resistance ohmic contact the barrier height must be low, and it is possible only if the interfaced materials possess relatively same geometric structures. In our case we are using four materials for contacts Ag, Cu, In and Al. The contact metals are deposited by the Nano-master Deposition System using the technique of physical vapor deposition also called the sputtering. A physical mask was used to pattern the top/backside contacts for Van der pauw Hall Effect measurements (surface), ASMEC (surface/bulk), and for the Transfer Length Measurements to check the contact resistance. After the formation of contacts, the readings are taken using the Hall Effect system and by the automatic system for material/device electro-physical characterization. The procedure for Hall measurements is the same as we discuss in the contactless except the one reading that is taken at liquid nitrogen environment to check the superconductive behavior of graphene. For hypersensitive surface and bulk characterization we used the ASMEC as completely

explained in chapter 4. The sample are placed in the prober for characterization as shown in Figure 4.5:

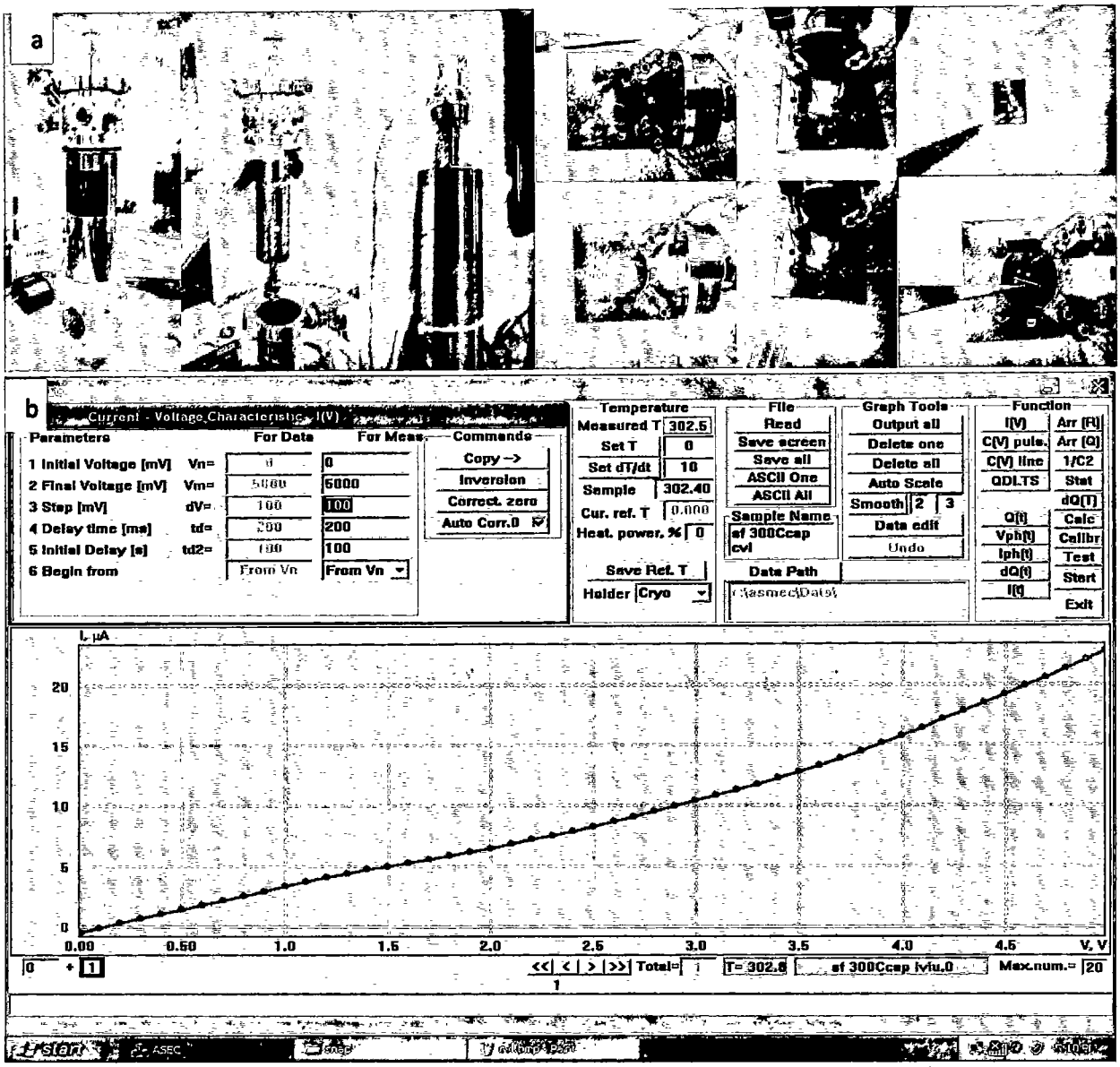


Figure 5.5: basic ASMEC procedure (a) sample placements (b) reading by built in software

5.4.3 TLM base experiment:

The transfer length method for contact resistance is briefly explained in chapter 4. Here we are going to discuss the experimental setup and procedure to carry out the experiments. As we know from the previous chapter that five metal pads of same size with variable distance were designed of sample surface. For electrical characterization we are using the Multi-Head Probe Station which consist of four probes two for current and two for voltage measurements as shown in Fig 4.6:

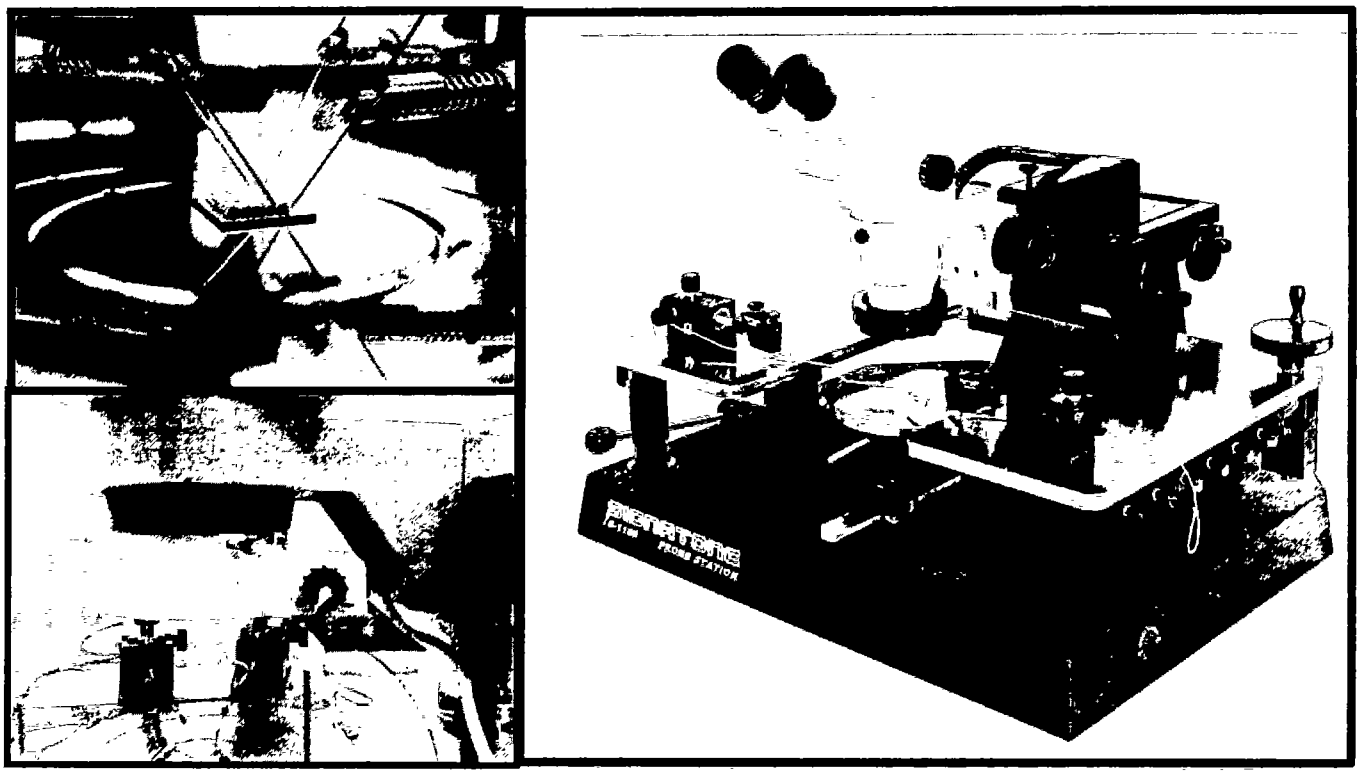


Figure 5.6: multi head probe station schematic for TLM measurements.

The resistance is measured w.r.t distance and plotted and from the TLM theory the contact resistance and sheet resistivity of target material can be find easily as discussed in previous chapter.

Chapter 6: Results and Discussions

In this chapter we are going to explain what we got from experiments. The details about experiments is explained in chapter number 5 quite briefly. Just a reminder as we have explained in thesis motivation section, the main objective of this project is to study the hypersensitivity of graphene interface with other material here in this case is the Ni. The structure we are using is known as graphene based transistor matrix grown by chemical vapor deposition method in which Ni is used as a catalyst to grow graphene layers. The transistor matrix is the basic building block for future graphene transistors.

The main goal is to study the hypersensitive electrical properties of graphene transistor matrix specially the hypersensitivity of graphene/Ni interface. As explained in previous chapter that we are using the Nano-chip reliability Grade Hall Effect system and the Van der pauw method for electrical characterization. In electrical characterization we are going to focus on 5 electrical parameters which has so importance related to hypersensitivity. The electrical parameters include

Rs (ohm/sq) =Sheet resistance

Rho (ohm-cm) =Electrical resistivity

Con (1/ohm-cm) = Electrical conductivity

Ns (/cm^2) = Carrier concentration

Mobility (cm^2/Vs) = Electron/Hole mobility.

We are dividing this chapter into two sections. In section 1 we are analyzing the effects of metal contacts on graphene/Ni interface and compare the results with contactless measurements. In section 2 we are going to anneal the samples at different temperatures

and compare the results with non-annealed samples. Also the sample will be characterized at cryogenic temperatures to study the superconductive nature of graphene.

6.1 Section 1:

In this section we are going to discuss different parameters related to Hall measurements without metal contact and with metal contact. The first parameter of importance is the sheet resistance. Sheet resistance of graphene is not unique and depends upon the interface material and the synthesis method. The interface material on which graphene is grown is of great importance due to its direct effect on graphene properties like sheet resistance. Actually sheet resistance here is like normal resistance because the length and width of the sample is same as 10×10 mm. The thickness of graphene layers is founded to be 1.43 nm by Spectroscopic Ellipsometer, which means that an average there are 4 layers of graphene on nickel surface. The van der pauw method is used for finding the sheet resistance of graphene/Ni interface structure. The lattice structure of graphene and Ni are relatively the same due to which there in strong covalent bonding between them. The high level interaction between graphene and Ni makes the separation distance as minimum of 0.21 nm [48] typically less distance than the wonder wall forces in graphite. This is some kind of doping in graphene and will change all related properties of graphene especially here the sheet resistance of graphene, which means that actually we are measuring the combine effect of graphene under the influence of Ni. Here we are using four different materials for contacts which include Al, Ag, Cu and In. For contact metallization we have used the thermal evaporator system having the following experimental parameters during metal vaporization as shown in table 6.1 below.

Source Material	Material Density	Material Z-Ratio	Pressure Torr max	Current	Deposition Rate	Thickness Achieved
Aluminum	2.73 g/cm ^{3}	1.080	10E-5	150 A	2.5 A/S max	50 nm
Silver	10.5 g/cm ^{3}	0.529	10E-5	146 A	2.5 A/S max	50 nm
Copper	8.93 g/cm ^{3}	0.437	10E-5	216 A	2.5 A/S max	50 nm

Table 6.1: experimental data/parameters for contact metallization

The work function of graphene is not constant and varies from 4.5-5.0 eV depends upon the growing technique and the number of layers stacked upon each other's. The work function of both graphene and contacted metal plays a key role to minimize the contact resistivity which limits the performance of graphene based electronics devices specially field effect transistors. The role of the work function becomes more obvious in case of metal/graphene interface structures in which the graphene high work function leads to increase the carrier transport efficiency from the metal electrode to graphene surface which generally considered to be the condition for ohmic contacts with negligible contact resistance/resistivity. S. M song et al, investigated the variation in graphene work function under the metal electrodes and its impact on contact resistivity. Their research was based on to find answers for some basic question about the graphene (1) is graphene under the metal is still graphene or it loses its unique properties? (2) Is the graphene work function remain the same under the interfaced metal? (3) Does high work function graphene interfaced with metal indeed provide the low contact resistance? (4) Is the work function of graphene interfaced with metal is the only reason for low contact resistance? On the basis of

their experimental results they answered the question as (1) Graphene under metal electrode is still graphene with some unique quantum properties (2) The work function of graphene is not preserved and changes metal to metal. It's sometimes pinned to the work function of the interfaced metal and sometimes to an intermediate value irrespective to contact metal (3) it is not guaranteed that the low contact resistance is due to the high work function of graphene (4) the work function is not the only factor that influence the contact resistance there are many other reasons which directly effects the contact resistance like the bonding type between graphene and metal, lattice mismatch and the inter-atomic distance between metal and graphene surface. In the light of the above discussion we have deposited 4 different metal contacts having different work functions and plot their effects on sheet resistance as work function is related to contact resistance.

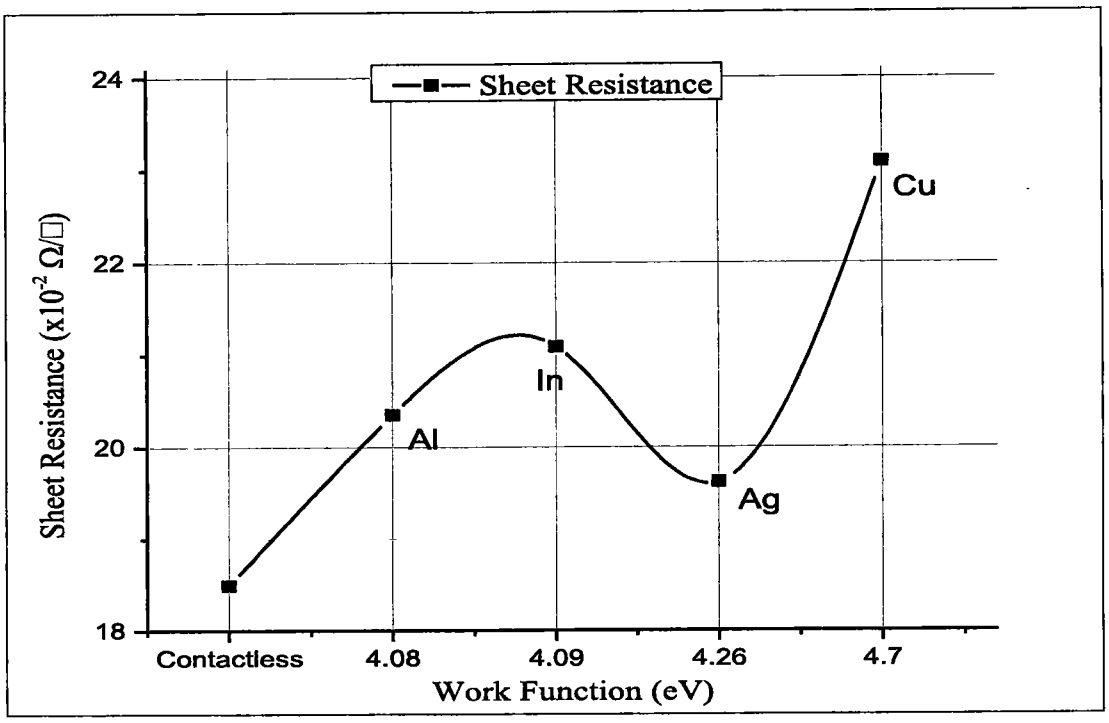


Figure 6.1: sheet resistance of graphene transistor matrix vs metal work function.

In the above Figure we see that without metal contact we have the minimum sheet resistance. Sheet resistant gradually increase when we deposit metal contact. As silver is a good conductor of electricity so the sheet resistance is minimum as we deposit silver contact. The highest sheet resistance we get when we deposit Cu contact on graphene transistor matrix as Cu and graphene has least solubility and diffusion profile and Cu is mostly used to grow monolayers of graphene. In this case the deposited metal thickness is kept constant (50 nm) to analyze the differences between them is terms of their effects on sheet resistance of graphene transistor matrix. The results show that 5 sample with different metal contacts are characterized and we get minimum sheet resistance when we deposit Ag and the highest sheet resistance is case of Cu as a contact material.

Next we are going to explain the difference between resistivity of graphene transistor matrix with metal contacts and without metal contacts as shown in Figure 6.2:

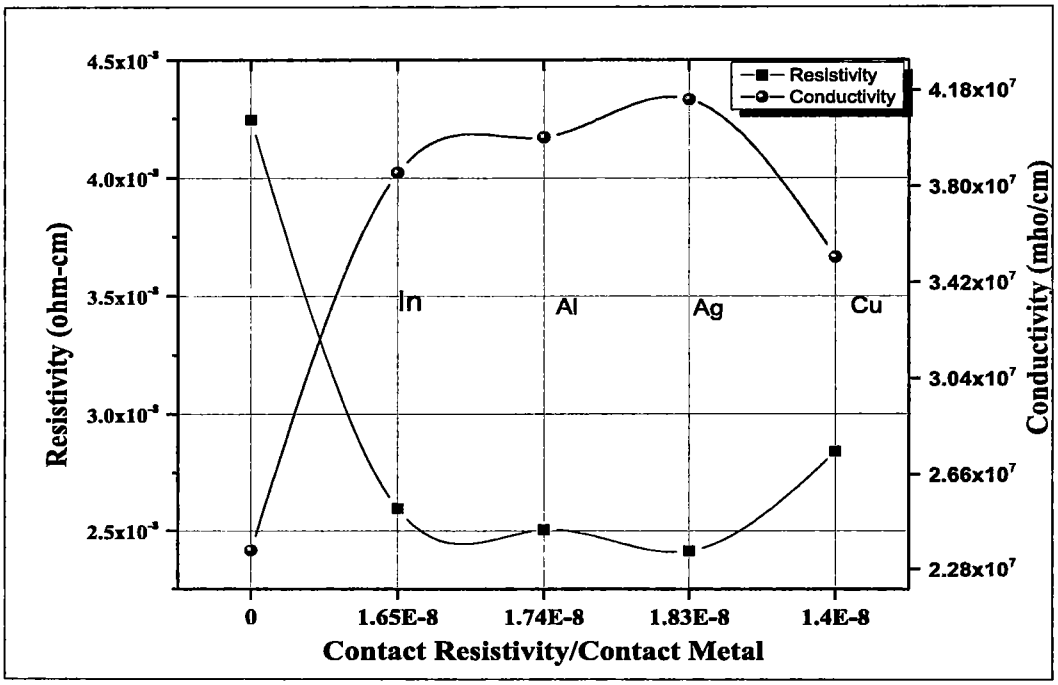


Figure 6.2 electrical resistivity & conductivity of graphene/Ni interface without and with contacts.

A. K. Geim el all in 2009 [49] find out that the resistivity of suspended graphene sheets is in the order of 10^{-6} Ω·cm while we see in the above Figure when graphene becomes in interface with Ni the combine resistivity drops to the orders of 10^{-8} Ωcm which mean that in terms of device fabrication point of view the graphene/Ni interface is quite important to get low resistivity. Next when we deposit different metal contacts on graphene surface we see that in case of silver contacts we have the lowest resistivity values and the highest in the case when we deposit Cu contacts, also keep in mind that the size and thickness of all deposited metal contacts are same. The converse will be a little bit different because in case of the electrical conductivity of the interface, because the highest resistivity yields to lowest conductivity as we clearly see in Figure 6.2:

Electrical conductivity is one of the most important property of graphene because intrinsic graphene is considered to be a superconductor at room temperature due to the longest mean free path (65 micron) for charge carriers. Considering the above Figure, we have minimum conductivity in contactless measurements while the maximum conductivity when we deposit Ag contacts. The conductivity of graphene is round about 1.00×10^{8} and that of Ni is 1.43×10^{7} while what we see in above Figure in case of silver contact that, the graphene nickel interface structure has the conductivity of 4.43×10^{7} which means that there is some sort of donated electron from Ni to graphene to improve the conductivity of graphene [50].

By definition carrier concentration is the number of charges in the conduction band or valence band. The intrinsic graphene carrier concentration of graphene is not too high but by stacking of graphene layer carrier concentration can be increased. Tian Fang et al, found

that the intrinsic carrier concentration of single layer of graphene at room temperature is 8.5×10^{10} cm^{-2} [51]. Now in case of extrinsic graphene the carrier concentration depends upon the interface structure of graphene with target substrate like Vincent E. Dorgan et al studied the multilayer graphene behavior on SiO_2 substrate and fined the carrier concentration to be 2×10^{12} cm^{-2} [52]. As we are using the graphene/Ni interface structure we get the highest values of carrier concentration as shown in Figure 6.3:

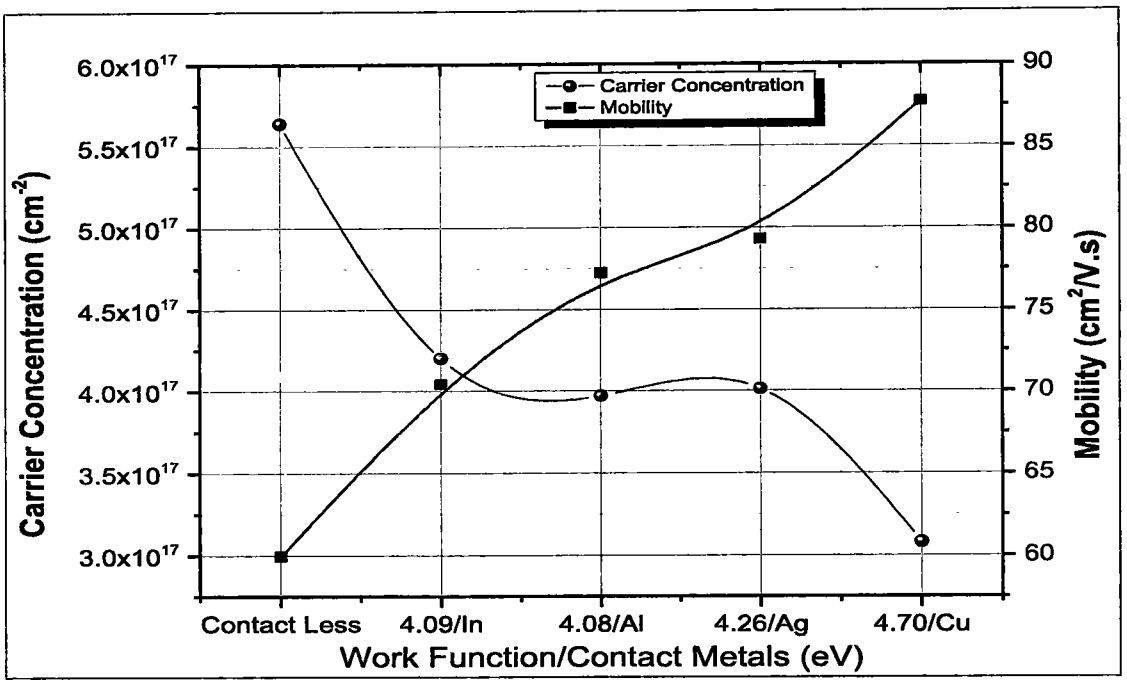


Figure 6.3: carrier concentration and mobility of graphene transistor matrix.

As we are using stacks of graphene over Ni substrate that is why we get the highest carrier concentration of 5.64×10^{17} cm^{-2} due to access charge carriers contribution of Ni substrate. Now the carrier concentration decrease when we deposit metal contact for electrical characterization and the minimum carrier concentration we found when we deposit Cu contacts on graphene transistor matrix as obvious from Figure above.

Suspended graphene has the highest electron mobility of 200,000 cm^{-2} /vs. [53] at low temperature unlike the semiconductors whose charge carrier becomes immobile at extreme low temperatures. The graphene mobility dramatically changes when graphene becomes in interfaced with insulating and metallic materials due to the charge puddle created by interface materials. In our case the graphene is interface with nickel which makes a chemisorption bonding destroying the honeycomb structure of graphene. The effects of this interface will be a decrease in mobility as shown in Figure 6.3 above. The reason for the less mobility includes the non-homogeneous thickness of graphene on nickel substrate during the fabrication process and also the ineffective modulation inside the graphene caused by the nickel grain boundary scattering. Due to these reasons we have a large variation in field effect mobility of graphene/Ni interface and ranges from 100 to 1000 cm^{-2} /vs. [54]. The metal contacts also have a direct effect upon the mobility as we see in the above Figure, in case of contactless measurements the mobility is quite low as compared to the contacted samples measurements. There is a lot of variation in graphene transistor matrix mobility with respect to the type of metal we are going to use as a contact material. In our case we have the highest electron/hole mobility when we used Cu as a contact material while the minimum value when there are no contacts.

6.2 Section 2(a): Annealing effects on graphene-metal interface:

The contact resistance at the metal-graphene interface is the major issue and the performance killer for graphene based transistor application. As discussed earlier that the contact resistance depends upon the bonding nature of metal-graphene interface. The value for contact resistance should be minimum for reliable operation of graphene based

transistor but due to contamination during fabrication like resist residue sandwiched during lithography or any other contamination may increase the contact resistance. Annealing of the sample is a post processing technique used to improve metal-graphene contacts and to minimize the contact resistance. In case of Graphene-Ni interface annealing produces extra carbon dangling bonds in graphene which leads to minimize the interface resistance and increases the carrier exchange rates.

To follow the industrial standards, we have annealed the samples for few seconds using the rapid thermal processing unit at different temperature. The deposited contacts metal includes Cu and Ag and the annealing temperatures varies from 300 to 400 °C for a fixed time of 60 seconds. The parameters of study are the same as for the previous experiments. For of all we are going to investigate annealing effects on sheet resistance of the graphene transistor matrix as shown in Figure 6.4 below.

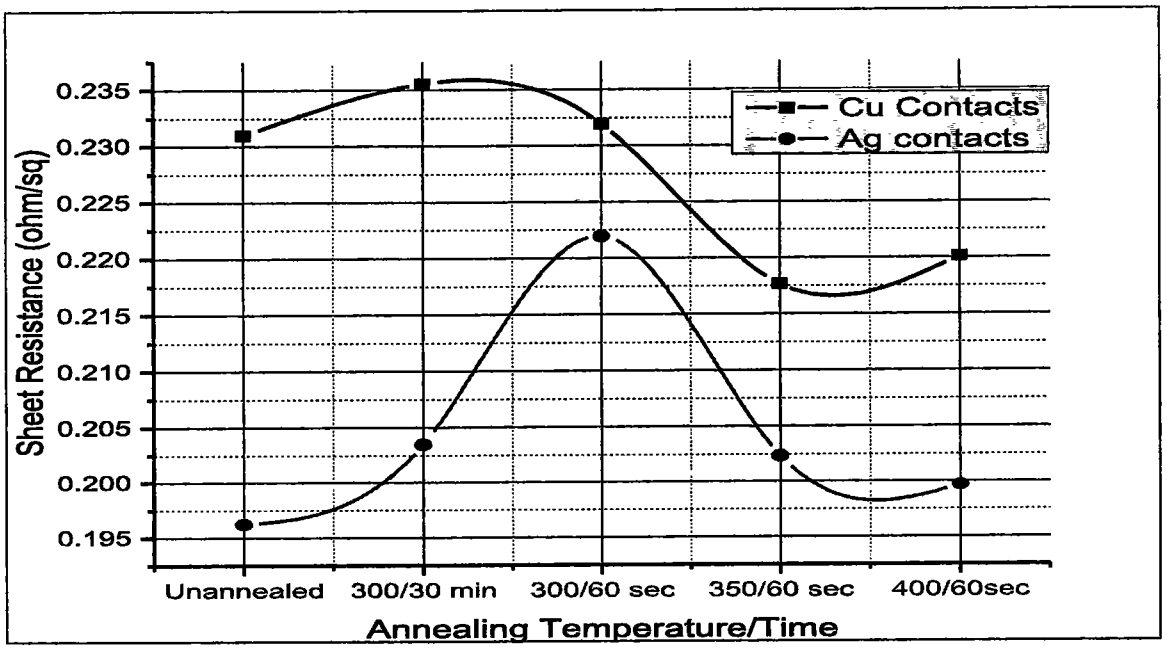


Figure 6.4: sheet resistance variation at different annealing temperature.

Figure 6.4 shows the variation in sheet resistance when we deposit two different metal (Ag, Cu) contacts and annealed the sample at different temperatures. As we see the sheet resistance is minimum in case of Ag contacts as compared to Cu contacts. The graphene/Ni interface is quite sensitive to temperature in case when we apply a rapid thermal energy budget to it, and there is a possibility of carbon atoms diffusion inside the Ni which may produce variation in graphene thickness causing the sheet resistance to vary. But as we are going to increase the annealing temperature the sheet resistance simultaneously starts decreasing which mean that we are getting the minimum contact resistivity.

Now in case of electrical resistivity of graphene/Ni interface when we deposit Ag and Cu contacts and anneal the sample at different temperature as shown in Figure 6.5:

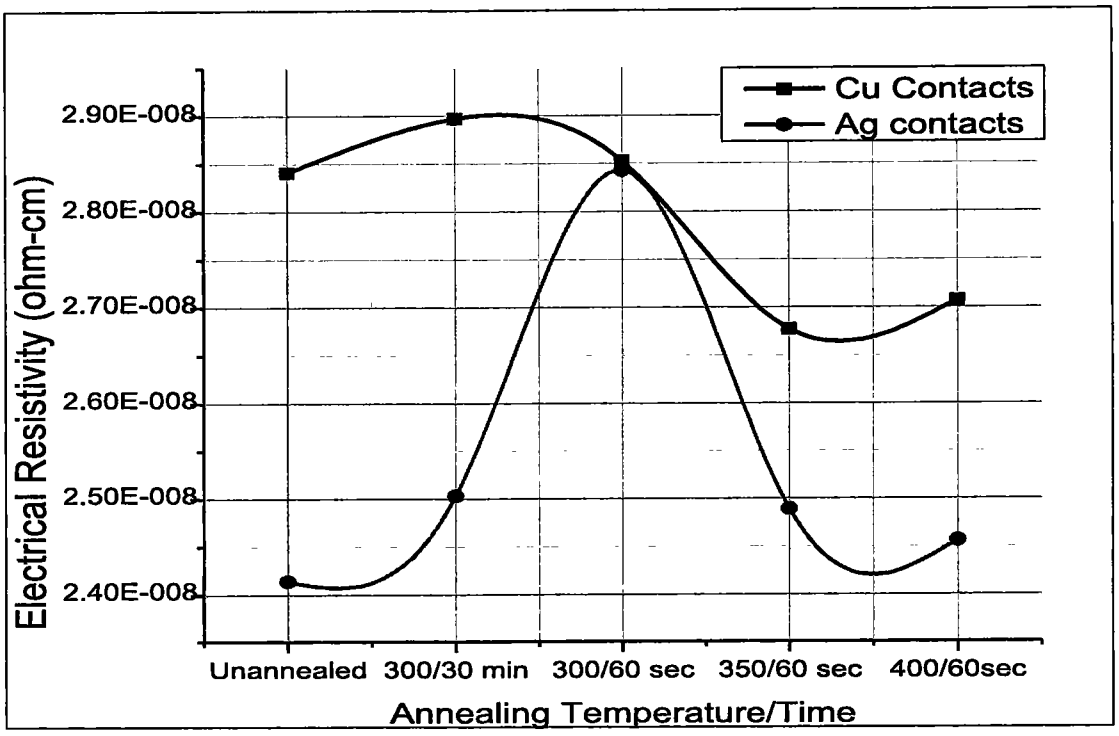


Figure 6.5: electrical resistivity of graphene/Ni interface at different annealed temp with Ag & Cu contacts

As we see from above Figure that the same sample have different electrical resistivity value when we deposit two different materials as a contacts also the different variation is observed at different annealing temperature. In case of Ag contacts, the electrical resistivity slowly increases at low annealing temperature while there is a continuous drop at high annealing temperature. Also in case of Cu contacts due to oxidation there is a continuous increase in electrical resistivity while at 300 °C both have relatively same impact on electrical resistivity of graphene/Ni interface.

The contact resistance plays a crucial role in the charge transfer between metal and graphene junction which means that by minimizing the contact resistance we can brought improvement in electrical conductivity as shown in Figure 6.6:

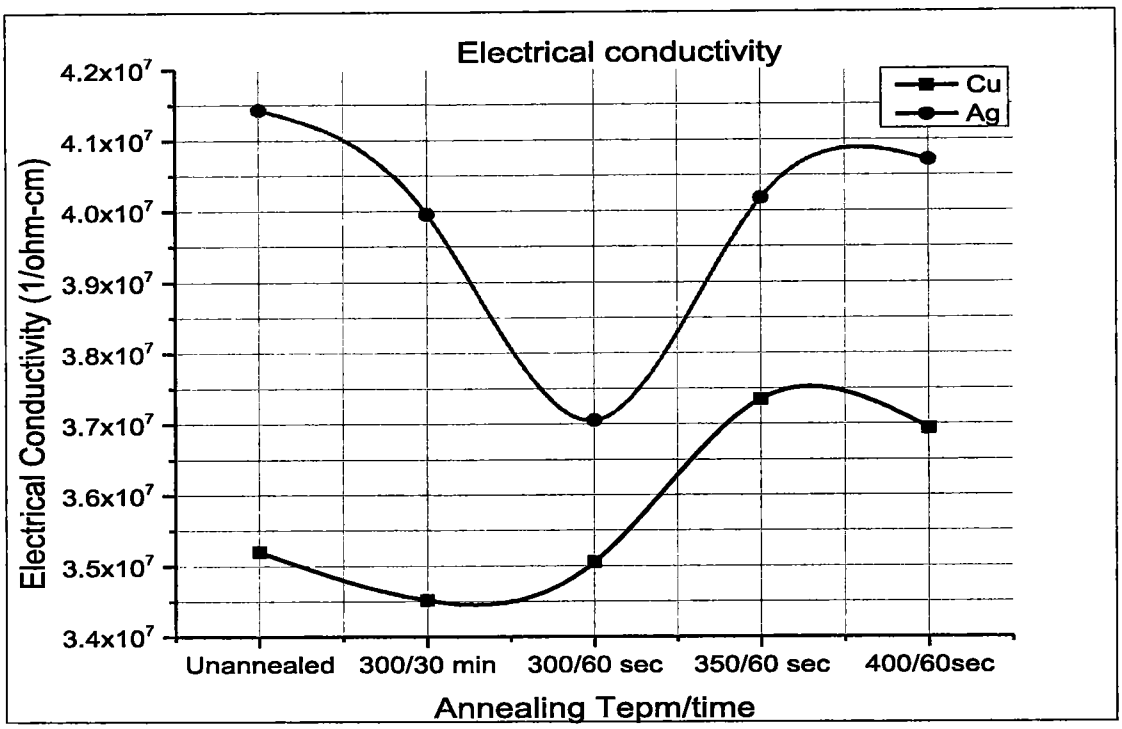


Figure 6.6: Electrical conductivity variation with different annealing temperature

As we have deposited two different metals (Ag, Cu) as a contact material and also annealed for a short and a long duration. The results in above Figure shows a continuous improvement in conductivity with respect to different annealing temperatures in the case of Ag as a contact material. For Cu the conductivity graph is a variable one due to the oxide formation at the edges of Cu contacts.

Before the metal contacts deposition, we have the carrier concentration of 5.64E+17 but after the contacts its certainly drops due to the metal/graphene interface resistance/contact resistance is shown in Figure 6.7 below

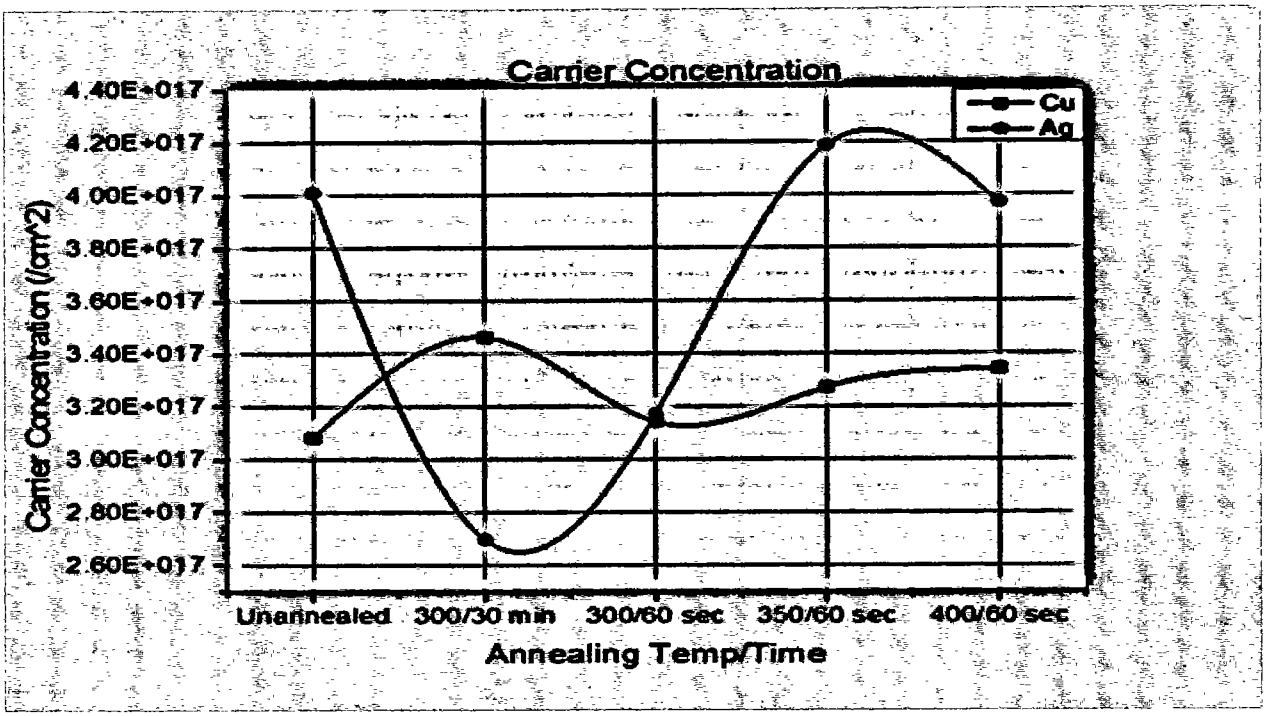


Fig 6.7: carrier concentration in terms of different annealing temperature when we deposit Cu & Ag contacts.

As obvious from the Figure the green line represents Cu contacts while the orange line represents the Ag contacts. Carrier concentration totally depends upon the interface mechanism between graphene and the deposited metal and the size of the contacts because

the charge carriers normally injected to graphene channel through a metal contact. So if the metal/graphene interface is not so strong is will causes the charge density de-pinning at the contact edge as we see in the above Figure 6.7 in case when we deposit Cu contacts.

Now in case for electron mobility when we deposited two different metals for contacts and then apply a constant thermal budget for 60 seconds. The changes are quite obvious in case of Ag contacts when annealed at 300°C as shown in Figure 6.8:

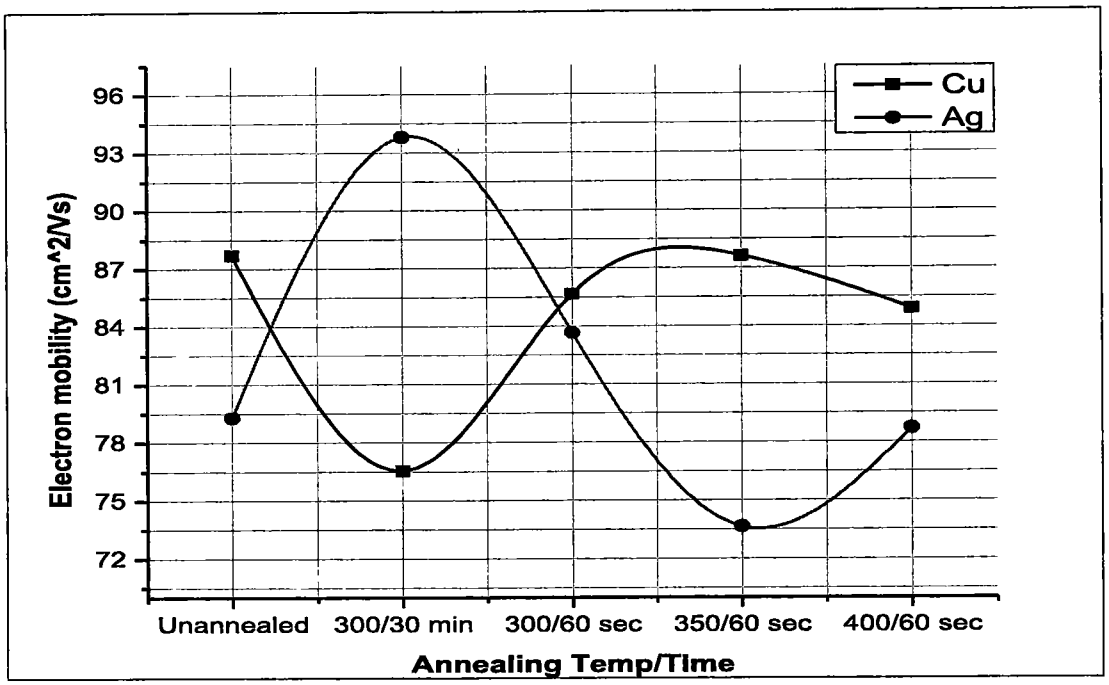


Fig 6.8: mobility variation of graphene transistor matrix at different annealing temperature when Cu and Ag is used as contact material

There are two main reasons for mobility improvements by rapid thermal annealing. No 1 is the decrease in contact resistance due to annealing as annealing removes any type of contamination sandwiched between metal graphene interface structure. No 2 is the grain boundaries issue as graphene grown by CVD method is polycrystalline in nature and contains numerous amount of grain boundaries/defects which is the main reason that we

are getting low mobility values. So by annealing we are going to realign the carbon atoms by applying thermal energy. The highest mobility of 93 $cm^2/(V \cdot s)$ we get for Ag contacted sample when annealed at 300 °C while in the case Cu contacts we get the mobility to 87 $cm^2/(V \cdot s)$ when annealed at 350 °C as shown in Figure 6.10 above.

6.2.1 Section 2(b): Graphene transistor matrix electrical properties at cryogenic temperatures:

In this section we are comparing the results obtained from Hall measurements conducts at room temperature vs the Hall Effect measurements conducted at liquid Nitrogen environments. Ag is used as a contact metal in case contacted measurements and the parameters of study are the same as discussed in previous results. First of all, we are going to discuss change in the sheet resistance of graphene/Ni interface when the samples are characterized at room temperature, at liquid nitrogen environment and annealed at different temperatures. Normally graphene shows a partial superconductor like behavior at cryogenic temperature and the sheet resistance becomes minimum at liquid nitrogen environment. In this section the change is sheet resistance is of graphene transistor matrix is measured at five different annealing temperatures. The temperature is varying from 77k to 673k and the results is shown in the form of Arrhenius plot in which the logarithmic value of sheet resistance is plotted vs the inverse of temperature. We see in Figure 6.9 that the Arrhenius plot is a straight line and the slope is representing the activation energy Ea which in our case is 17.17meV. The activation energy is the minimum energy required for a device to bias.

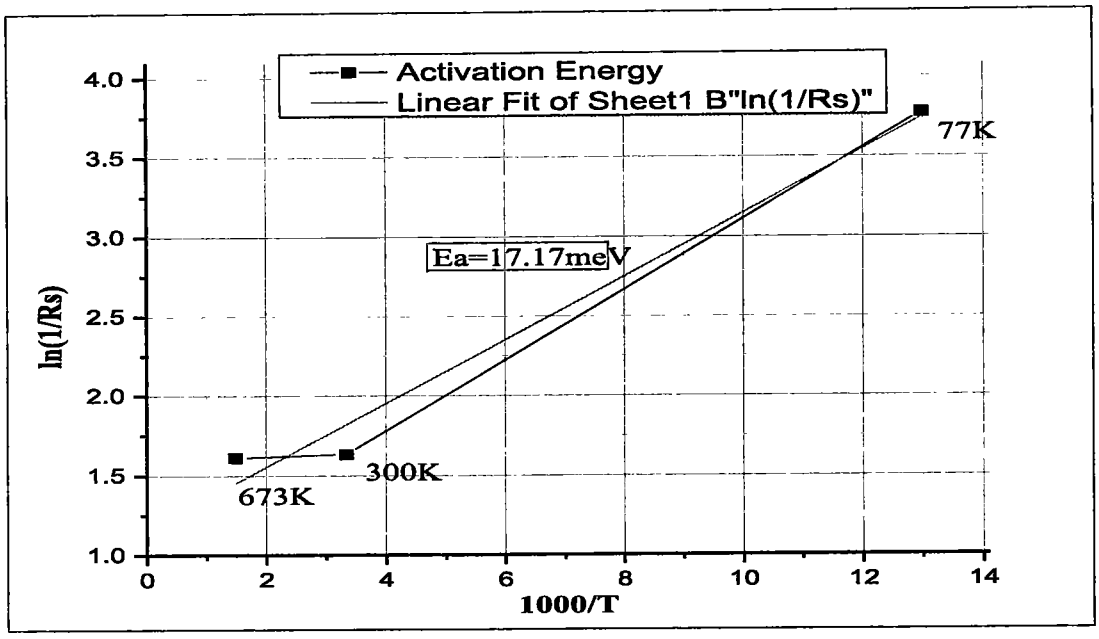


Fig 6.9: comparison report in terms of sheet resistance at various temperature conditions

As we see in Figure 6.9 experiments are conducted at different environmental condition and the difference in sheet resistance is obvious for each condition. At cryogenic temperature we have the minimum sheet resistance which shows the superconductive behavior of graphene/Ni interface. The sheet resistance increases when we deposit metal contacts on graphene transistor matrix due to the contact resistance between metal/graphene interfaces. The 16 h in LN means that the sample was dipped in liquid nitrogen for 16 hours and after that we characterize its electrical properties to check the effects of extreme low temperatures on graphene transistor matrix.

Normally the resistivity of an intrinsic semiconductor decrease with increase in temperature while the converse is true for metal in which the resistivity increases with increase in temperature. Graphene is a semi-metal and interfaced with Ni so here we a kind of residual resistivity due to Ni interface as shown in Figure 6.10:

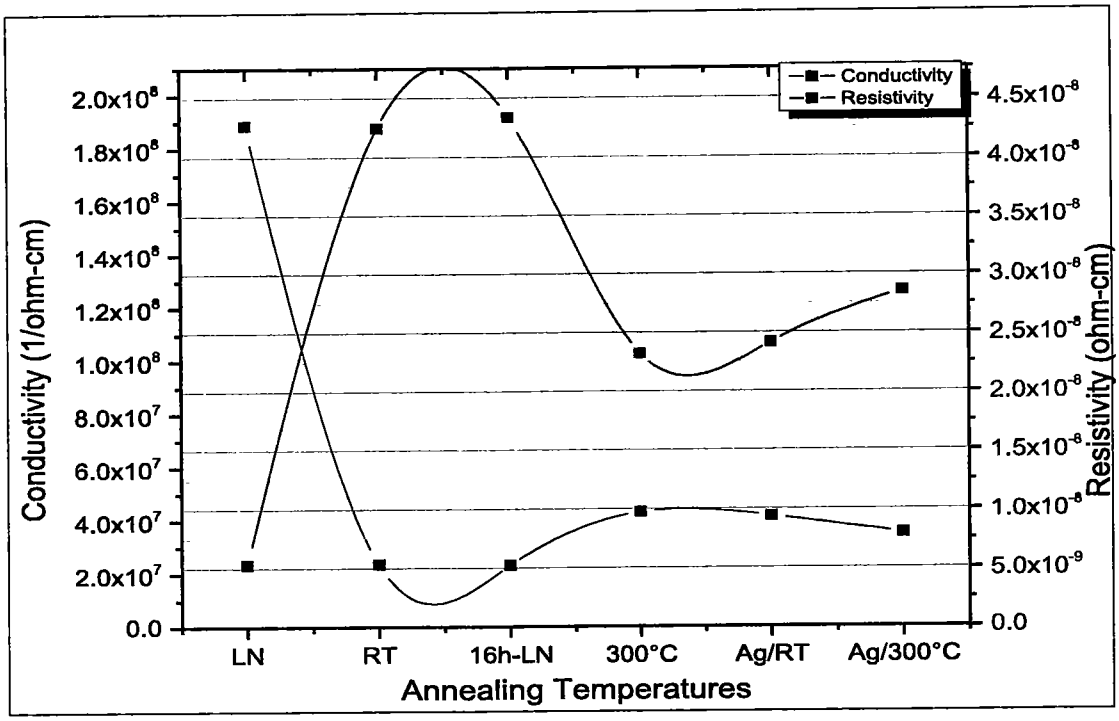


Figure 6.10: the electrical resistivity & conductivity at 77k vs room temperature.

The comparison shows that we are getting less resistivity value at cryogenic temperature and then the resistivity increase with increase in temperature as shown in the readings taken a room temperature. The converse is true in case of electrical conductivity because we are getting the highest electrical conductivity at cryogenic temperature as shown in Figure 6.10.

The reason for high electrcial conductivty is the minimum collision ratios between electron-electron and electron-phonon at cryogenic temperature and also the electrical conductivity is independent of charge carrier density at extreame low temperatures. The conductivty of graphene may be effected by the interface defects/charge impurities and also the contact resistance may incrase at liquid nitrogen enviroments due to the contraction of metal surface interface with graphene.

The carrier concentation increased at crogenic temperature due to the ambipolar transport

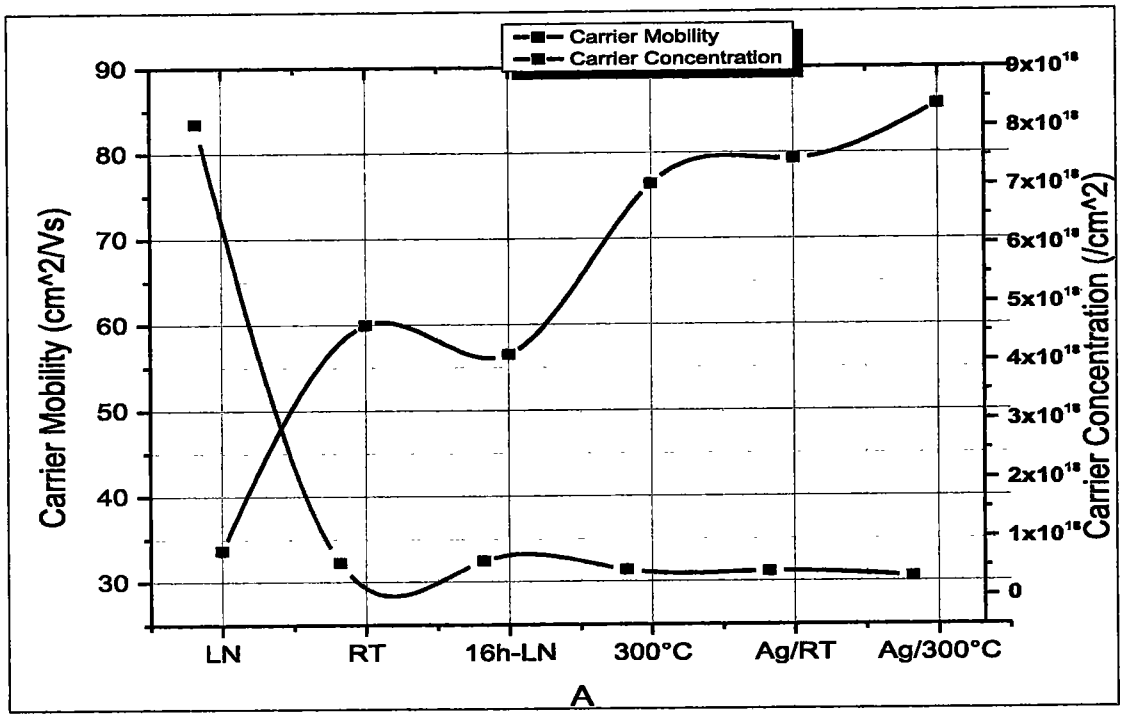


Fig 6.11: carrier concentration & mobility of graphene transistor matrix on different temperatures

In graphene because holes and electron both can be charge carriers. Holes can be converted into electron and electron can be converted to holes by applying electric potential and also by low temperature. In Figure 6.11 the carrier concentration is maximum at cryogenic temperatures due to the lack of bang gap ingraphene. The carrier concentration value drops due specific contact resistance (tunneling effect) when we deposited metal contacts.

Suspended/free standing graphene behaviors like a superconductor at cryogenic temperatures because the graphene mobility is increased with decreased in temperatures irrespective the large number of charge carriers. In some cases, the graphene behaves differently especially in case of interface structures of graphene with other material may be metal or a dielectric material which limits the graphene mobility. The limiting factors includes the Coulomb's scatterings, short range scattering, underlying substrate surface phonon scattering and the charge puddle produced by the different grain size. In case of

graphene/Ni interface the grain boundaries inside the Ni as well as graphene creates the charge puddles to trap the charge carrier and degrades the mobility. The cryogenic mobility of graphene/Ni interface structure is shown in Figure 6.11:

In Figure 6.11 we see that at room temperature we have the elctron mobility of 60 $cm^2/V{\cdot}s$ which certainly drops to 33 $cm^2/ (V{\cdot}s)$ when the sample is characterized at 77k. Next compare to cryogenic mobility when we deposit metal (Ag) contacts and characterize the sample at room temperature the mobility improves and we see much more improvements in the case when we anneal the sample by minimizing the contact resistance.

6.2.2 Section 2(c): Arrhenius Analysis.

In this section we are going to discuss the Arrhenius analysis by finding the activation energy which is the minimum energy required for conduction. First of all, the metal contacts in this case silver is deposited using the thermal evaporator system after that the I-V curves are taken at different temperatures ranging from 300k to 350k by ASMEC. The resultant of I-V graph is the resistance of graphene transistor matrix which is plotted vs temperature. We observe an inverse relation of resistance with temperature as with increase in temperature the resistance decrease and vice versa. The percentage change is resistance in resistance vs temperature is plotted in Figure 6.11:

From the Figure we see that the percentage change in resistance is increasing with temperature which means that the resistance is decreasing which leads the current to increase.

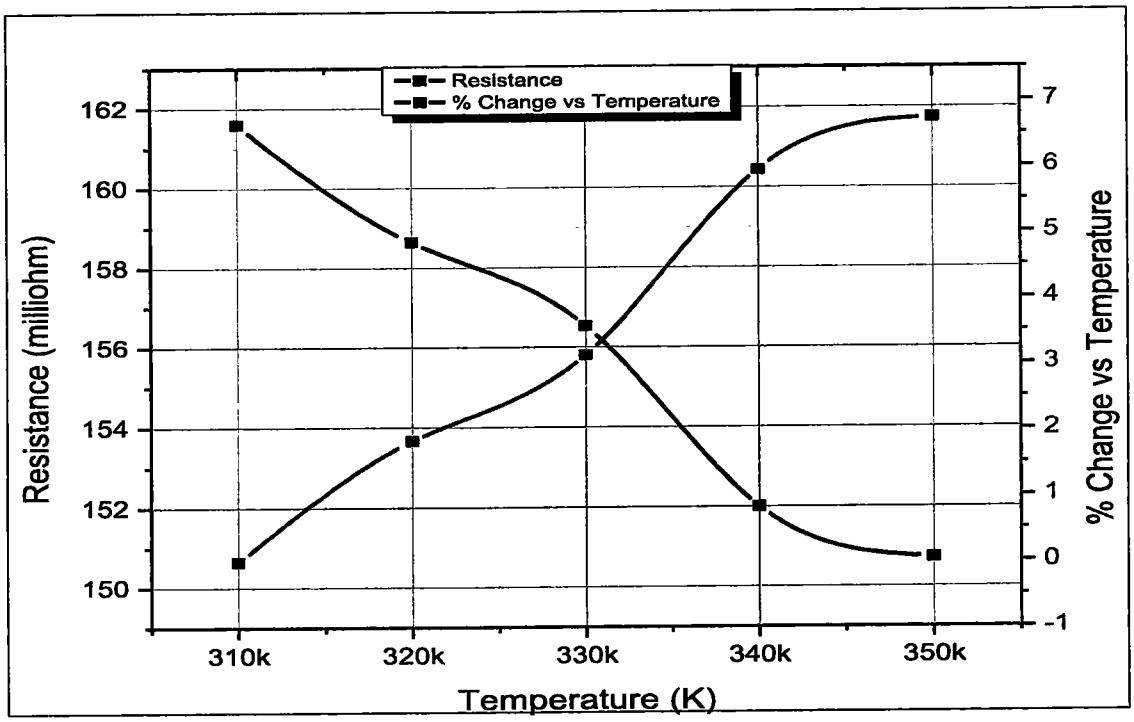


Fig 6.12: Resistance vs temperature (black line), Temperature vs %change in Resistance (blue line).

Next we are going to plot the Arrhenius plot of conductivity vs the temperature to find the activation energy using the Arrhenius equation given as.

$$\sigma = \sigma_0 \exp\left(-\frac{E_\sigma}{KT}\right)$$

Where σ0 is pre-exponential factor, Eσ is the activation energy and k is Boltzmann constant whose value is 8.6173303×10^{-5} eV K^{-1}. As we have discussed in early chapters that graphene boundaries acts as a traps for charge carriers so the minimum energy required to set free

these charge carriers is the activation energy sometimes called the thermionic or thermal activation energy which plotted in the Figure 6.13 below.

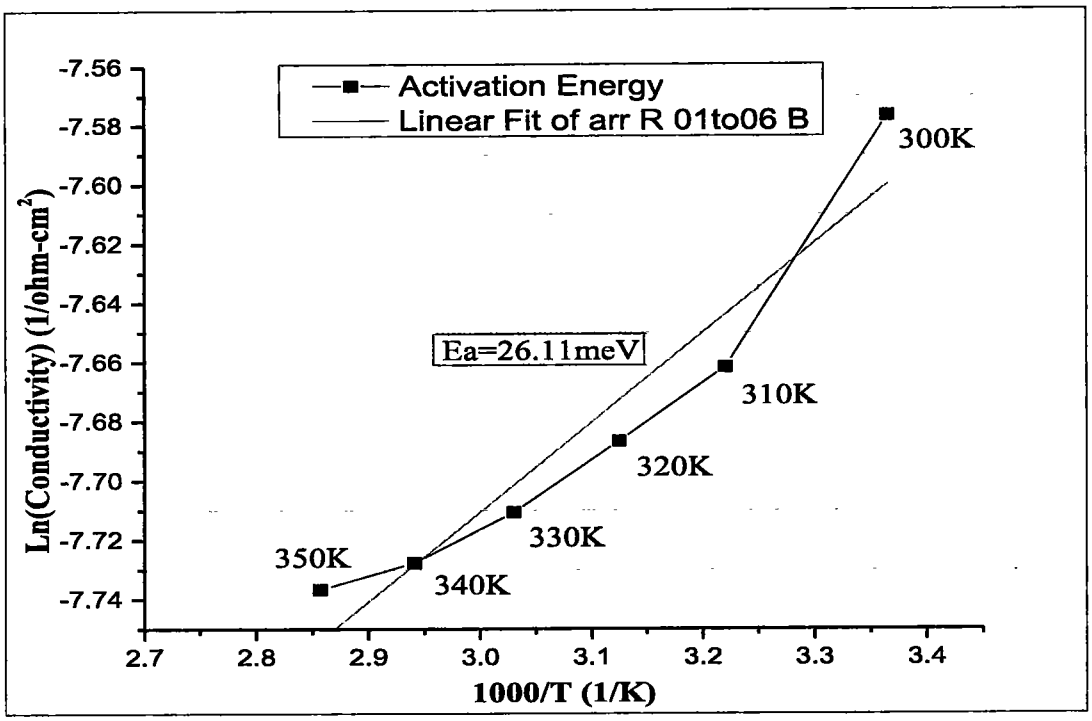


Fig 6.13: The 1/T dependency of conductivity of graphene transistor matrix

The activation energy is found to be 26.11 meV by linear fitting which means that the minimum energy required for charge carrier to conduct is the 26.11 meV which is the activation energy of the system. By comparing to the activation energy find by N. Prasad et al [55], which is 16.2 meV we have an incremental value because they characterized graphene on silicon dioxide surface while in our case the interface material is nickel. The increase in activation energy is due to the large grain boundaries in graphene as well as in Ni surface. To minimize the grain boundaries, we have annealed the sample at various temperature and reduced the activation energy up to 17.17 meV.

Chapter 7: Summary and Further Work

7.1 Summary and key findings:

In this thesis we have investigated the hypersensitive electrical properties of 2D graphene based transistor matrix. As we know the electrical transport measurements through the graphene/Ni interface structure needs metal contacts so for this purpose we have deposited 4 different metal contacts having different work function which includes Al, In, Cu, Ag of same thickness and area. Studies revealed that the nature of graphene/metal bonding is of two types the chemisorption and the physisorption. The chemisorption bonding is observed in case of graphene/Ni interface structure in which the Ni destroys the hexagonal structure of graphene and as a compensation to the damage created it donates an extra electron/atom to graphene which leads us to the fermi level pinning and doping of graphene. The deposited 4 metals make a physisorption bonding mean in this case the unique properties of graphene transistor matrix are preserved and only the physical dynamics of the metal/graphene interface are responsible for any change in electrical characterization which can be overcome by various techniques to get better results. The key finding is listed as follows

[1] For all the deposited metal contacts the ohmic nature is observed with the specific contact resistivity in the order of 10^{-8} Ωcm^2 lower than 10^{-6} Ωcm^2 which is the basic requirements for ohmic contacts.

[2] The contact resistivity of metal/graphene interface is mostly independent of the metal work function but in some cases like Ni the highest work function values leads us to

minimum contact resistivity values due to the major work function difference w.r.t graphene but most of the times it depends upon the physical dynamics of the metal/graphene junction.

[3] Ag is found to be the best contact metal as we have observed the minimum sheet resistance and electrical resistivity in the case when we deposited Ag as contact material which leads us to highest values for electrical conductivities and carrier concentration.

[4] Interfacial doping is observed due to the chemisorption bonding between graphene & Ni as electron transfer due to work function difference which leads us to the band gap opening in graphene.

[5] The activation energy of the system is found to be 17.17 meV at room temperature while 26.11 meV at elevated temperature which is the proof of band gap opening in Ni doped graphene matrix as activation energy is the minimum energy required for a charge carrier transition from donor level to conduction band.

[6] The Hall mobility is quite low due to the excess number of charge carriers as well as the structural defects in CVD growth method like grain boundaries, non-uniform thickness and point defects.

[7] A superconductor like behavior is observed at cryogenic temperatures regime due to the lowest resistivity and sheet resistance values at cryogenic temperatures.

[8] Rapid Thermal Annealing is found to the best post-processing technique to minimize the contact resistivity as well as the grain boundaries in graphene.

7.2 Future outlook:

The unique electrical, optical, mechanical and magnetic properties of graphene make it a greatest contender for future electronic application. Graphene is optically more transparent than the ITO currently used in touch screen panels and also it flexibility will make graphene in future to replace the ITO. Graphene is also the strongest material ever discover so in future the graphene composites can be added to other material to increase their electrical, optical and mechanical capabilities. Other future graphene application includes the energy application like graphene batteries, Fuel cells, super capacitors, graphene membranes, graphene sensors. In this research we have investigated the hypersensitive electrical properties of graphene because graphene is thought to be the future silicon of semiconductor industry. As we have discussed earlier that suspended graphene possesses some extra-ordinary properties like high electronic mobility, ballistic transport of charge and many more, but somehow when graphene is becoming in interface with other material its properties changes dramatically specially in the case of graphene/metal interface. In the graphene/metal interface case the contact resistance is considered to the performance killer for graphene field effect transistors in which the graphene is used as a channel material in contact with metal electrodes. The interface is not the only issue in our research we also find that the quality of graphene we are using is not very good as it contains variation in thickness as well as the grain boundaries which means that there is still a gap in terms of a suitable method to grow high quality graphene at industrial level.

The main reason till now about graphene usage in a logic device is the absence of band gap. But without bandgap graphene can be used as fastest interconnects between electronics and

light wave's devices. To open a bandgap in graphene it will need a little bit ingenuity like doping, graphene ribbons have built in band gap or by using the graphene property of negative resistance. The future of graphene based electronic devices is totally depended upon the growth methods and the quality of graphene with minimum defects and to do so we will need a well establish industrial standard method for graphene synthesis.

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