Simulation, Fabrication and Characterization of Ultra Shallow Junction in CMOS

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A thesis is submitted to

Department of Physics

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Final Approval

It is certified that the work presented in this thesis entitled "Simulation, Formation and Characterization of Ultra Shallow Junction in CMOS" submitted by **Rehana Mustafa**, Registration No. 6-FBAS/PHDPHY/S10 is of sufficient standard in scope and quality for the award of degree of PhD Physics from International Islamic University, Islamabad

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Department of Physics

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CERTIFICATE

It is certified that Rehana Mustafa Registration No. 6-FBAS/PHDPHY/S10 has carried out the research work related to this thesis titled, "Simulation, Formation and Characterization of Ultra Shallow Junction in CMOS" under our supervision. This work fulfills all the requirements for the award of the doctor of philosophy.

(Prof. Dr. Ahmed Shuja Syed) **(Prof. Dr. Ehsan Ullah Khan)**

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Abstract

CMOS being heart of today's electronic industry has been under rigorous research and development. International Technology Roadmap of Semiconductors (ITRS) is placing stringent process requirement in order to meet the issues in scaling of these devices as well as predicting the future of Moore's law. Ultra-shallow Junction (USJ) formation is getting critical both in terms of physical dimensions and consequent device characteristics exhibited once the protocol is adopted in CMOS or Transistor-based nano-scale architecture. We have performed a range of experiments on doped Silicon substrates and created a processing strategy to form USJs in nano-devices having physical dimensions ranging from 10 and 60 nm in several cases. A systematic study of their pre- and post-process simulation on trade-off simulators has been carried out. Structural, optical, electrical and surface characteristics of variety of these pre- and post-processed devices have also been performed and presented in order to provide a realistic assessment on the direct and indirect junction depths, their stability and possible usage in industry.

Chapter No. 1

1.1 Introduction

Complementary Metal Oxide Semiconductor (CMOS) is the most widely used integrated circuit design. It is found in almost every electronic product from hand held devices to mainframes. CMOS uses PMOS and NMOS transistors wired together in a balanced fashion that causes less power to be used than NMOS or PMOS transistors by themselves [1]. CMOS and bipolar transistors are used in combination for many applications. In semiconductor materials and devices, region in which two materials featuring distinctly different electrical properties are in contact is called a junction; e.g. p-n junction and metal-semiconductor junction (contact). Depth (measured from the surface) of the plane in p-n junction at which concentration of acceptors is equal to the concentration of donors is called junction depth. In either P or N-type substrate if the dopant elements attain deep locations in the substrate, then the junction formed will be deep but if these dopant atoms remain near the surface of the substrate than the junction formed will be called a shallow junction. According to ITRS roadmap, transistors with ultra shallow junction are essential requirement for getting high speed devices (gigahertz) [1, 2, 3].

The depth of these junctions is usually controlled by controlling energy of the implanted ions and setting of appropriate RTA annealing temperatures. By scaling down CMOS its performance can be improved in terms of power dissipation and switching time and it has a remarkable feature that as it becomes smaller it also becomes cheaper, faster and enable more functions per unit area of a silicon chip. As a result it becomes able to provide superior performance at reduced cost per function.

The main focus of the thesis is to simulate and fabricate the ongoing protocol to form nano-scale ultra shallow junctions in standard silicon CMOS. These ongoing protocols are the processing sequence (implantation followed by the annealing) already calibrated and matured to the industrial requirements. We have re-visited several such protocols and simulated the established scheme on more than one

modified computer code and verified existence of junction at different annealing temperatures.

The research in this work becomes relevant and commercially viable particularly for post-implant annealed ultra shallow junction protocols. None of the simulation packages currently in use at global fabrication facilities for the batch production of CMOS devices, which incorporates the effects of in-situ annealing (beam heating) during the implantation process as well as the dynamic annealing to electrically activate the junctions. Therefore, it becomes important to look into the modeled data loosely and compare it with the post-annealed schedules. The effect of damage production and subsequent annealing out relatively at high degree thermal treatment is crucial to take into account whenever a new protocol is being established. We have performed and compared these results in order to model and estimate the extent of accuracy in newly developed protocols for USJ formation in nano CMOS devices.

Main parameter that are kept in mind throughout this research work are; (a) To have an abrupt junction, Formation of these junction at minimal reduced depth. (b) To achieve minimum sheet resistivity. (c) To have maximum dopant activation in the selected area.

1.2 Scope of the Thesis

This research involves the fabrication and characterization of ultra-shallow p^+/n junctions for ultra-large scale integration technologies. For the formation of ultra-shallow junctions, silicon substrates were first preamorphized by Si^+. Indium and carbons are than co-implanted by using low energy ion implantation and in second set boron ions were then implanted using ultra-low energy ion implantation in n-type silicon. Both types of samples were than post annealed between temperature regimes 600-800°C. The ultra-shallow junctions were mainly characterized using, Hall Measurement System, Keithley 4200, CV Measurement System, Ellipsometry, Rutherford backscattering spectrometry (RBS), Grazing Incidence X-Ray Fluorescence (GIXRF), XRD and Atomic Force Microscopy to study the impact of implantation energy and post annealing temperature on dopant depth, electrical

1.3 Objectives of the Thesis

The primary goal of this thesis is to achieve highly doped and electrically activated ultra shallow junctions (USJs) with suppressed sheet resistance at different annealing temperatures by using low thermal budget RTA. To achieve the primary goal of this work, the studies will be carried out in different sections associated with their own specific objectives described as follows:

1. In order to find out the resultant range and damage profile in the Si due to Indium and Carbon ions, we performed rigorous simulations with various ion energies at different incident angles' using a computer code Stopping and Range of Ions in Matter for the present work. Further, Silvaco TCAD code was used to predict the distribution of defects in the Si substrate due to the carefully chosen ion implant schedules. These simulations constitute the central part of the research work, because very careful parameter optimization is required to study the process sequence to fabricate ultra-shallow junctions.
2. Samples were fabricated on the basis of these simulation results.
3. Samples activation and junction formation was checked for further processing.
4. Only those samples were further processed in which junction was established and electrically activated.
5. To determine the effect of ramp-up rates on dopant redistribution, samples were post annealed (RTA) between temperature regimes 600-800°C.
6. We have investigated for both pre- and post-annealing process to create a processing strategy for potential applications in nano-devices. For this purpose as-implanted and post annealed samples were than characterized to study the effects of annealing temperature on dopant profile (junction depth, sheet resistance, mobility, absorption coefficient, refractive index, strain and surface morphology) with those obtained before and after annealing temperature.
7. The formation of junction and its depth is verified by different techniques.

1.4 Organization of the Thesis

The organization of the thesis is highlighted as below;

Chapter 1 covers some introductory information pertaining to the subject matter of this study. **Chapter 2** describes necessary background of the simulation and experimental tools used for the synthesis and characterization of the samples. **Chapter 3** provides the comprehensive Literature Review on the subject while the experimental details are provided in **Chapter 4. Chapter 5** contains results and discussions and analysis of these results. **Chapter 6** This chapter summarizes the major results and findings, and provides conclusions based on these findings in the light of the objectives of this research. Recommendations for further experimental work are also given.

Chapter No. 2

2.1 Description of Physical Phenomenon and background Physics

2.1.1 Shallow and Ultra Shallow Junctions

CMSO (Complementary Metal Oxide Semiconductor Field Effect Transistor) is the semiconductor technology used in the transistor that are manufactured into most of today`s computer microchips. Semiconductors are made of silicon and germanium, material which "sort of" conduct electricity, but not enthusiastically. Areas of these material that are "doped" by adding impurities become full-scale conductors of either extra electron with a negative charge (n-type transistors) or of positive charge carriers (p-type transistor) [1,2]. A CMOS semiconductor uses both NMOS (negative polarity) and PMOS (positive polarity) circuits. In CMOS technology, both kinds of transistor are used in a complementary way to form a current gate that forms an effective means of electrical control. CMOS transistors use almost no power when not needed. This makes them particularly attractive for use in battery-powered devices, such as portable computer. Personal computers also contain a small amount of battery-powered CMOS memory to hold the date, time and system setup parameters. As the current direction changes more rapidly, however, the transistors become hot. In integrated circuit technology, millions of instruction can be executed in a single second [2].

A CMOS based chips has impurities added to it, a process called "doping", such allows the chip to store an electrical charge called capacitance. In order to control the electrical currents needed, the capacitance must be discharged and recharged which takes time and causes the transistors on the chip to heat up. This production of heat, limits the speed at which microchips can operate. For this reason microchips have poor yield rates. SOI microchips are not doped with impurities, which eliminates such of the capacitance and allows an SOI microchip to operate faster and cooler and it was found that for this silicon oxide film is perfect enough that it bonds with the pure crystal silicon layer [3].

The word junction is used in solid state electronics is a common region comes in mind that is situated between n and p-type materials and due to this junction, depletion region is formed. It is achieved by having either p or n type substrate and doping it with opposite species. If the dopant elements attain deep location in the substrate, then the junction formed will be in that corresponding depth. But if these dopant atoms remain near the surface of substrate, then junction will also be formed, but this type of junction will be known as shallow junction. A junction just below the surface of the substrate will be known as Ultra shallow junction (USJ). But in all aspects depth should be maintained to such extend that there should be no effects of it on device operation due to some unavoidable parameters. Also as devices are having USJs, their dimensions are reducing which means less consumption of power and more advantage in technology. Device should have minimum sheet resistivity, thus providing ease for carriers to flow in device; there should be sufficient number of active dopant carrier in the device to support the flow of the charge. The junction is called abrupt junction when the concentration of the dopants is constant on both sides of the junction and changes instantly at the junction [4].

2.1.2 Simulation Techniques

During the last decade, numerical modeling of the semiconductor fabrication process has increasingly become an important design and development tool in semiconductor technology. Development of a new or improved semiconductor device runs through a number of distinctive phases. In the first phase there is the initial design of the new device including the first setup of the fabrication process. Mostly options from already well-established processes and technologies are taken to form the initial new process. After this first design the process undergoes an optimization loop.

There by the process is tuned and improved to reach the specification and device characteristics. Finally, the process is ready for manufacturing, where impacts of manufacturing changes on performance and yield calculation are taken under investigation. In all these phases' simulation tools can play a crucial role for the reduction of the cycle time for device prototypes. A modern integrated circuit (IC) process consists of several hundreds of single process steps. The goal of process

simulation should sow be the full characterization of the most critical parts by means of numerical simulation tools [5].

Apart from being valuable in development and optimization of IC fabrication process, process simulation are necessary to predict accurate impurity profiles for subsequent use in device simulator programs. With the decreasing scale of the device dimensions there is growing demand for process simulator that account for multi-dimensional effects and accommodate more realistically the physical behavior during process of the device. The process models have to fulfill the requirement on accuracy, reproducibility, and predictability even in the development phase, because of the large manufacturing chain. From the process simulation point of view there are still process steps, such as cleaning, which need not be simulated, because their influence on subsequent process steps is insignificant or can be included in the next process step. The simulation task for process simulation can be reduced to the critical structural and impurity related process steps [6]. To model the experimental results, the process simulators used in this research are described below.

2.1.2.1 Simulators used for implantation optimization (SRIM & SUSPRE)

Two international simulation packages (computer codes), naming industrially trade-off IBM`s Stopping & Range of Ion in Matter (SRIM) and Surrey Ion Beam Center`s "Surrey University Sputter Profile Resolution from Energy" (SUSPRE) introduced by Ziegler. J. F, 2008 are used in this work [7]. In these packages different input parameters can be set in order to achieve required doping profile. In general by changing the value of each input parameters such as energy, fluence (dose) and angle of incidence of the incident beam simulation plots can be achieved showing various output parameters of the implantation which are steady state broadening, on set for amorphization, sputtering yield, erosion rate, nuclear and electrical energy deposited, mean range and standard deviation from SUSPRE. By SRIM 2008 the output parameters are collision plots in the form of longitudinal and lateral directions, ion distribution, lateral distribution, ionization n, phonons, and energy to recoil and vacancy requirements such as specified depth attained by dopant ions for ultra-shallow junction and implantation energy for minimal damage event created by ion beams etc [8].

2.1.2.2 Simulator used for Process optimization (TCAD)

Simulator for Technology Computer-Aided Design (TCAD) is already a fundamental part of silicon industry and has largely promoted the development of silicon-based devices [9]. As optoelectronic devices are gaining importance in daily life appliances, simulator for their simulation analysis play a significant role in the near future. Today, several simulators for lasers have been released to the market but they are still challenged when dealing with the complicated devices like VCSELs. At the very beginning, Senturus, which is released by Synopsys, Inc., was chosen for this work.

2.1.3 Ion Implantation

A non-thermal method of introducing impurities into Silicon is called ion-implantation. In this process doping atoms are ionized, accelerated and directed at the Silicon wafer. The high-energy ions enter the crystal lattice, collide with the Silicon atoms and finally come to rest. The energies required in this process are in the range from a few keV to MeV and for the commonly used impurities such as Boron [10, 11] Indium, Carbon [12] Arsenic [4] and Antimony etc., this process can be used to implant ions from a depth of few nanometers to 10-1000 nm beneath the Silicon surface [11]. The acceleration energy control the average depth of the dopant atoms in the silicon and ion current during implantation controls the ion dose. Therefore to form a very shallow dopant layer, low energy implanters are needed. Ion implantation has become important because of its ability to control, with precision, the thickness and doping level of implanted layers by the energy and dose of the ion species [1].

Initially ion implantation was developed as a mean of doping these semiconductor elements of integrated circuits. It has several advantages over growth or diffusion techniques, such as accurate dose, depth control, good uniformity, reproducibility of doping, low temperature or room temperature operation, minimal lateral spread of dopants beneath a mask, and several dopants may be added. It is also often possible to introduce dopants, which cannot be introduced by diffusion. Because of the speed, accuracy, cleanliness and controllability of the process, it has become the standard for this type of work [13]. There exist several sources of evidence on the effect

that pre-amorphization enable obtaining better electrical activation of the dopants [14]. When all of the dopants being incorporated within a fully amorphized region above the position, where End of Range (EOR) defects would occur, this in turn allows more dopant atoms to occupy substitutional sites. By annealing at low temperature, dopants diffusion and probability of clustering can be minimized [15]. Ion implantation has become a routine method for the introduction of impurities into semiconductors [16].

This technique involves the production of positively charged ions, which are accelerated through a controlled potential and then allowed to impinge on the sample. Unlike diffusion methods, ion implantation allows independent control over the depth and concentration of the dopant. The main side effect of the technique is the production of a damaged layer because of the disturbance of the lattice introduced by the collisions induced, these damaged layers or defect can be removed using different annealing techniques. Due to the easy implementations of this technique, the microelectronic and nano-electronics devices industry has been extensively adopted it in the production from the last few years. Especially in the area of integrated circuit fabrication, it has become the dominant technology, for example in the production of CMOS devices.

2.1.3.1 Ion Stopping and Range

When an energetic ion enters a solid it loses energy through interaction with the electrons and nuclei of the target atoms. There are two basic stopping mechanisms by which energetic ions can be brought to rest. They are nuclear and electronic collisions [17]. In the first one kinetic energy is transferred to the struck atom, with the considerable deflection of the trajectory of the bombarding ion. At high velocity, or more precisely high incident energy, the nuclear effect is negligible and the electronics losses dominate the slowing down process. In the second one, the energy will be transferred to the electrons of the target atoms, and the ion will suffer no or negligible deflection. The sum of the two mechanisms gives the total stopping power (S). The usual expression for it is given in equation 2.1 [17]:-

$$S = (dE/dx)_n + (dE/dx)_e \qquad (2.1)$$

Where dE/dx is the energy loss per unit path length of the ion. By the evaluation of the stopping power and its integration it becomes possible to find how far an ion will travel

inside the target before losing all its energy and coming to rest at some depth. The relative importance of the two mechanisms of stopping is well described in figure 2.1. In the usual cases of implantation for device fabrication the typical used range is between 10 to 200 eV. This energy window falls at the left of the figure where mainly the nuclear stopping mechanism takes place.

Both the stopping mechanism (electronic and nuclear) contributes to the energy loss of the incident ion inside the target. The ion once implanted follows a random path as it moves through the target. The total path length in Silicon is composed of a mixture of horizontal and vertical motion and is called Range (R). The projection of the range in the vertical direction (normal to the surface implanted) is called the Projected Range (R_p). Considering the large concentration of ions introduced during the implantation process (usually larger than 10^{12} ions /cm^2), it is possible to consider that (R_p) represents the average depth of the implanted ions. The distribution about that depth can be approximate as a Gaussian centered at (R_p) and with a standard deviation (σ) [18]. With this assumption the ion concentration n(x) as a function of depth will have the following expression:-

$$n(x) = n_0 \exp\left[\frac{-(x-Rp)2}{2\sigma 2p}\right] \qquad (2.2)$$

Obviously this model is an approximation and the real distributions differ from it. To take into account those differences justifying the discrepancies between this real profile, other parameters such as Skewness and Kurtosis can also be considered [18]. When the implantation target is solid with crystalline structure the impinging ion can move through particular direction such as atoms rows or planes, so that it travels long distances without undergoing nuclear collisions. Ions are steered down these channels by glancing collision with the atoms rows or planes. Hence they can travel through the solid longer distances resting eventually at deeper position. This phenomena is known as channeling and it is responsible for an asymmetrical final implant distribution inside the target resulting in a tail on the deeper side of the distribution [19].

2.1.3.2 Implant Damage

While ion implantation allows an accurate dose of impurity atoms to be placed on a controlled distance from the surface of the substrate, it has the disadvantage of introducing damage to the material. When the high energy ions collide with the substrate they displace the substrate atoms from their positions in the crystals lattice. In addition only a small number of the implanted impurities end up in the electrically active lattice sites. As seen, an in its path along the atoms array of the solid target bombarded, loses its energy in different ways (nuclear or electronic collisions) reaching finally a resting position.

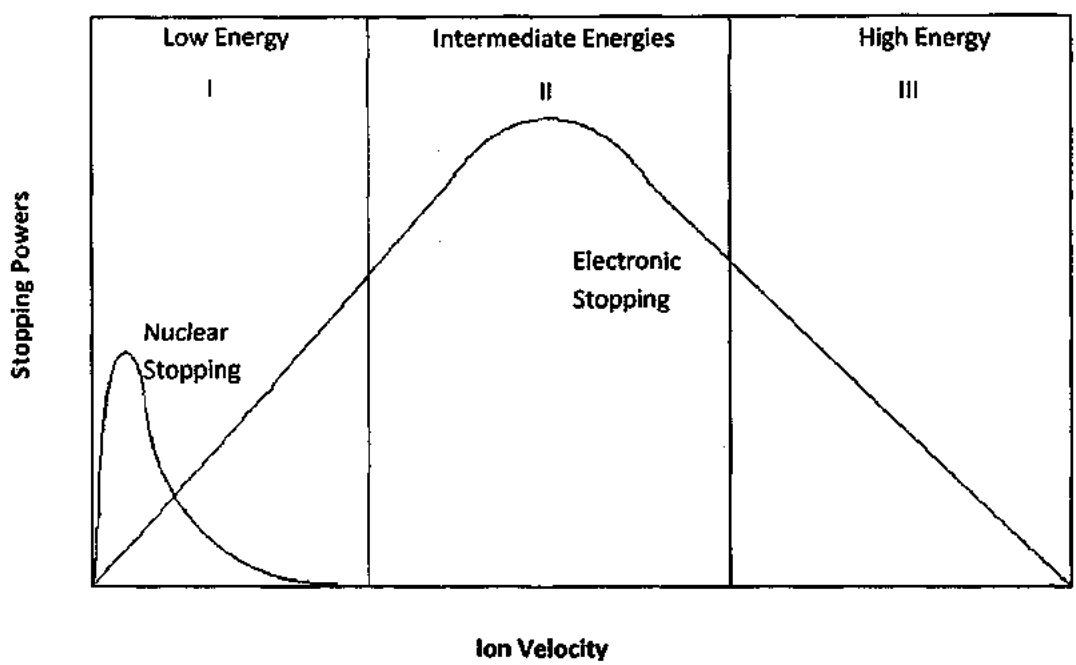


Figure 2.1: Relative amount of nuclear and electronic stopping power as a function of ion velocity.

In the case of electronics the energy lost by the ion is transferred to the target producing ionization or electronic excitation with consequently photon and thermal emission. In the nuclear scattering regime the effect is different. Since the binding energy of a lattice site is only 10 to 20 eV [20], so it becomes quite easy to produce displacement of the target atoms. However both ions and displaced atom have enough

energy to produce further displacement traveling through the target. The energy is spread over many moving particles resulting in the process called collision cascade. The overall result is the production of (vacancies) missing atoms in lattice positions and (interstitials) atoms resting in the lattice position producing a substitutional impurity. Implanting heavy ions into a light target results in a denser cascade with a resulting defects structure very different from the other extreme (light ions in heavy target). In the first case when the heavy ion (like Indium or Antimony) impinges on a surface of Silicon the deflected ion continues into the lattice accompanied by a primary recoil atom. Both of them could possess enough energy to produce other displacement in the following collisions. The ion energy shared between a numbers of atoms recoiled and the ion impinging will produce a collision cascade having a cylindrical form with its axis on the path of the ion. As the energy of primary ions decreases the fraction of energy transferred to lattice atoms increases. The recoil density will increase as the ion penetrates deeper in to the solids, until the ion energy will not be able to promote the displacement of lattice atoms. The disordered region produced by all the ions implanted will result in the production of a background zone of simple defect structures and a distribution of larger, disordered region.

The ion energy has an important effect on the amount of damage induced. In fact only nuclear scattering damages the target and is a function of the ion energy. However, for a given energy the heavier the ion implanted the larger will be the nuclear stopping power and consequently the more damage is produced [18].

2.1.4 Annealing

As an ion travel through the target it undergoes a series of nuclear collisions. Every time the ion is scattered a fraction of its energy is transferred to a target atom, which is displayed from its original position. The binding energy of a lattice site is only 10 to 20 eV [20], so it is easy to transfer enough energy to free an atom from its position and make it travel through the target as a second projectile. So both the ion and displaced target atom travel and cause further displacements. Eventually the energy becomes too small and the cascade stops. But after many ions have been implanted an initially crystalline target will be so disturbed that it will be changed to a highly

disordered state. Annealing is then required to repair the damage and put dopant atoms on substitutional sites where they will be electrically active. The success if often measured in terms of the fraction of dopant, which is electrically active however the challenge is not simply to repair the damage and activate the dopant, but to minimize the diffusion.

The time and temperature cycle of the heat treatment of implanted samples, known as the annealing cycle. It has a significant influence on the sitting of implanted impurities within the host substrate lattice. It is the installation of impurities within the host lattice, which determine the resistivity and consequently the conduction properties of the material. The concentration of activated impurity atoms is a function of the implanted dose as well as the annealing cycle. The goal of the post implant annealing is to restore the silicon lattice to the pre-implant state and to electrically activate the implanted dopant atoms. Since most implanted dopants do not occupy substitutional sites upon implantation [21]. A thermal step is required to provide the energy required to move the atoms to the correct lattice site. Electrical activation of the dopants in an amorphous layer proceeds differently from the activation of dopants within primary crystalline damage. Electrical activation in amorphous layers occurs as the impurities are incorporated into lattice sites during recrystallization [21, 22].

Electrical activation in areas of primary crystalline damage proceeds with more complexity. The movement of doping atoms according to a dopant gradient in a semiconductor material is called diffusion. It occurs during any high temperature processing steps, either as intentional or as parasitic effect. Due to the requirement of very shallow junction in modern semiconductor technology, diffusion is mainly a parasitic effect of the annealing step after ion implantation or of an oxidation step which is performed at high temperatures [21]. Nevertheless there are still applications in the (well) formation in complementary metal oxide semiconductor technologies or the in-diffusion of dopants from a chemical vapor source. There are strong variations in the diffusivity of different dopant species. Besides, diffusion can be enhanced by oxidation or retarded by nitridation, because these processes generate point defects at the surface. These surfaces generated point defects as well as implantation induced point defects can have a strong influence on the diffusivity because they facilitate complex diffusion

mechanism like transient enhanced diffusion [22]. At high concentration levels the dopant can form non-mobile cluster or precipitates which decrease the average diffusivity. The exact control of all diffusion mechanism is a very critical issue during the manufacturing of a semiconductor device because redistribution of the dopants significantly influences the electrical characteristics. When clustering and precipitations of dopant concentrations above the solid solubility limit (SSL) are introduced into the crystal lattice, a portion of the diffusion atoms appears to be electrically inactive at room temperature. As dopant concentrations above the SSL are common in today's technologies, we have to take into account the clustering phenomena for the simulation of the dopant diffusion [23]. Types of annealing used in this research work are Rapid Thermal Annealing (RTA) and furnace annealing:

2.1.4.1 Rapid Thermal Annealing (RTA)

Rapid Thermal Annealing (RTA), also referred to as Rapid Thermal Processing (RTP), is the most popular technique used today to activate dopants following ion implantation. The system configuration can vary greatly. However, for shallow junction formation the goal is the same: rapidly heat the wafer to a high temperature (600-800°C) for a short time (a few seconds or less). Lower temperatures for such short time result in little dopant activation and insufficient damage removal. The time the wafer is held at peak temperature is often referred to as the soak time. A popular type of RTA is a spike anneal. This involves ramping the wafer up to peak temperature and then ramping it down, holding it for only a few milliseconds at peak temperature. The ramp-up rate and minimum hold time at peak temperature is limited by the system configuration. Two common configurations are the lamp-based system and the hot-walled system. Since the process involves heating the whole wafer, the wafer is ramped up from 600-700°C where it is held for a few seconds before ramping up to peak temperature. This reduces the effects of stress that develops in the wafer due to thermal gradients and layers with mismatched lattice constants. Unfortunately, the hold at 600-700°C increases the thermal budget of the process. Also, since the whole wafer is heated, and cools by radiative cooling. [24]. Slow cool-down rates also add to the thermal budget seen by the wafer. In current mainstream IC processing heat treatment is achieved by

means of large, hot-wall ovens in which wafers are processed. In RTP, only the relatively small thermal mass of the wafer itself is heated to and cooled from the processing temperature. The walls of the reaction chamber are water-cooled and remain at room temperature. The windows are air-cooled or water-cooled. Consequently, process steps may need only ten seconds for completion. A wide variety of arrangement for heating wafers in RTP systems with infrared and/or visible light have been designed and built. Figure 2.2 represents a diagram of generic RTP system. The wafer is supported by three quartz pins, which contact the wafer near its edge (omitted from figure) and heated by lamps or lamp array, which is separated from the chamber by a transparent window. Light passes from lamp array to the wafer through the upper window. The lower window can be used for remote measurement of wafer temperature or for application of ultraviolet light to the wafer. Power requirements for the lamp array are typically from several to several tens of KW [25].

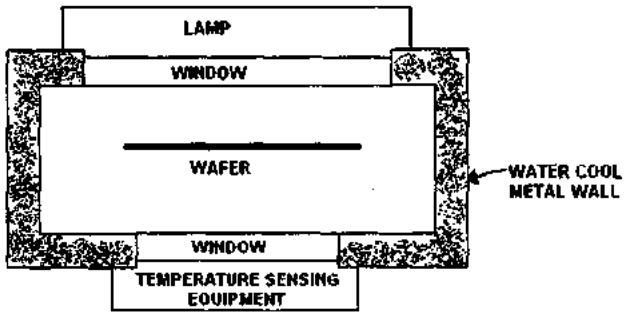


Figure 2.2: A Generic RTP system [25].

The advantages for the RTP system is the lower thermal budget, better process repeatability and shorter high temperature processing time for the wafer. However, since the wafer is very far from being in thermal equilibrium with its surroundings, the problem of temperature non uniformity over the wafer is much more acute. During the IC manufacturing silicon wafers undergo a number of processing steps typically at high temperatures under various atmospheric conditions, and high levels of heat power. However the control techniques required to provide real-time monitoring. One of the major problem is the control of the wafer temperature since it is required to maintain near uniformity temperature distribution over the wafer at all times, while following

fast temperature trajectories. A lot of research has been done to solve the non-uniformity problem. It is necessary to measure the temperature at various points across the wafer during RTP for multivariable control. The most popular approach is the use of pyrometers located outside the chamber. Recently there have been some new techniques developed such as double-pass infrared transmission and multi wavelength imaging pyrometer [25].

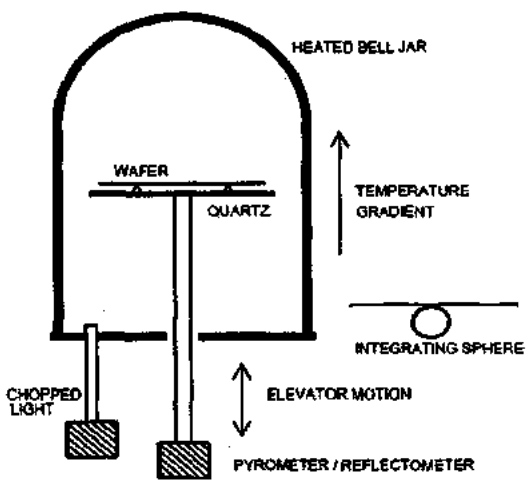


Figure 2.3: Furnace bell jar method, Emissivity corrected pyrometer uses reflectometers with in-situe chopped light and ex-situe integrating sphere [26].

2.1.4.2 Furnace Annealing

A bell jar furnace method for annealing implant monitors was developed at High Temperature engineering and improved with an emissivity compensating temperature measurement scheme [26]. Figure 2.3 shows a rough schematic. The wafer, on a support platform, is elevated into a heated zone with a vertical temperature gradient. The maximum temperature at the top of the bell- jar is set to be about 200°C above that of the desired process temperature. The comparatively weak sensitivity of wafer temperature to wafer emissivity within the near blackbody environment at high temperature has made this a viable method for open loop operation in some production.

Elevator motion is sufficiently fast to produce thermal spiking with 0.5 sec dwell time within 2°C of peak temperature. Under closed loop temperature control with

pyrometer focused on the backside of the wafer, some of the vest results for process reproducibility and uniformity have been claimed. The pyrometer for the bell jar method detects the thermal energy flux emitted by the wafer and measures the emissivity of the wafer. Emissivity, E is defined for practical purposes as the ratio of thermal emission received from the wafer relative to that of a blackbody at the same temperature [27]. The operating wavelength of the pyrometer about 0.95 μm is above (in energy) the Si band gap [21], where optical transmission through the wafer can be neglected [21]. An expression derived from energy conservation and the Kirchoff's law, which reduces to E=1-R, is used to compute emissivity from a separate measurement of reflectivity, R. the reflectivity is determined by mapping geometrical and background reflection factors as a function of elevator height and then normalizing bi-directional reflection signals to separate existed precision measurement of R at room temperature using hemispherical illumination. Wafer temperature is then computed from the Planck radiation law and a gauge factor for the detector sensitivity.

2.1.5 Theory of Electrical Characterization Technique

The following three techniques were used for the electrical characterization of our samples. In the following, brief introduction of these techniques is described.

2.1.5.1 Hall Measurement Technique

Hall Effect measurements are used in many phases of the electronics industry, from basic materials research and device development to device manufacturing [29]. A Hall Effect measurement system can actually be used to determine quite a few material parameters, but the primary one is the Hall voltage (VH). Other important parameters such as carrier mobility, carrier concentration (n), Hall coefficient (RH), resistivity, magneto- resistance (R), and the conductivity type (N or P) are all derived from the Hall voltage measurement [28, 29, 30]. With the addition of some other instruments, I-V characterization curves can be created with a similar test setup. Hall Effect measurements are useful for characterizing virtually every material used in producing semiconductors, such as silicon (Si) and germanium (Ge), as well as most compound semiconductor materials. They are equally useful for characterizing both low resistance

materials and high resistance semiconductor materials, including semi-insulating GaAs, gallium nitride (GaN), and cadmium telluride (CdTe) [29].

2.1.5.1.1 History of Hall Effect

The history of the Hall Effect begins in 1879 when Edwin H. Hall was working on his doctoral degree at Johns Hopkins University in Baltimore, Maryland discovered that if a thin gold plate is placed in a magnetic field, which is at right angles to its surface, an electric current flowing along the plate can cause a potential drop at right angles both to the current and the magnetic field termed the Hall Effect [30]. In order to determine both the mobility and the active dose, both resistivity measurements, similar to 4PP, and Hall measurements are needed. The Van der Pauw technique is widely used in the semiconductor industry to determine the resistivity of uniform samples and is used in this work. The Hall Effect can also be used to determine the carrier type (electrons or holes). The primary drawback to Hall Effect is the difficulty of forming ohmic contacts on high resistivity samples such as those with very low dopant concentrations. It is also highly sensitive to electrical defects [29].

2.1.5.1.2 The Hall Effect and the Lorentz Force

The basic physical principle underlying the Hall Effect is the Lorentz force. When an electron moves along a direction perpendicular to an applied magnetic field, it experiences a force acting normal to both directions and moves in response to the force and the force affected by the internal electric field [31]. For an *n*-type, bar-shaped semiconductor as is shown in figure 2.4, the carriers are predominately electrons of bulk density, *n*. It is assumed that a flow of current, *I* was along the x-axis from left to right in the presence of a z-directed magnetic field. Electrons subject to the Lorentz force initially they drift away from the current line toward the negative y-axis, resulting in an excess surface electrical charge on the side of the sample. This charge results produced the potential drop across the two sides of the sample (Note that the force on holes is toward the same side because of their opposite velocity and positive charge). This transverse voltage is the Hall voltage V_H and its magnitude is equal to IB/qnd,

where, I is the current, B is the magnetic field, d is the sample thickness, and q (1.602 x 10^{-19} C) is the elementary charge.

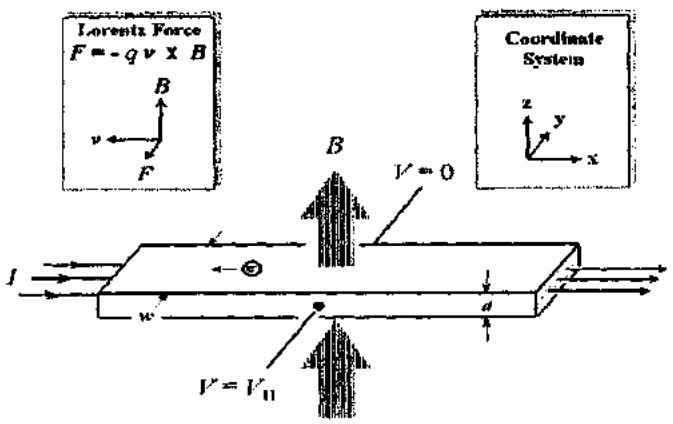


Figure 2.4: Schematic of the Hall Effect in a long, thin bar of a semiconductor with four ohmic contacts. The direction of the magnetic field B is along axis and the sample has a finite thickness, d.

In some cases, it is convenient to use layer or sheet density (n_s = nd) instead of bulk density:-

$$n_s = IB/q|V_H| \qquad (2.3)$$

Thus, by measuring the Hall voltage, V_H and from the known values of I, B, and q, we can determine the sheet density, n_s of charge carriers in semiconductors. The Hall voltage is negative for n-type semiconductors and positive for p-type semiconductors. The sheet resistance, R_S of the semiconductor can be conveniently determined by use of the van der Pauw resistivity measurement technique. Since sheet resistance involves both sheet density and mobility, we can determine the Hall mobility from the equations:-

$$\mu = |V_H|/R_S IB = 1/(qn_S R_S) \qquad (2.4)$$

$$\mu = R_H/R_S \qquad (2.5)$$

If the conducting layer thickness d is known, we can determine the bulk resistivity ($\rho = R_S d$) and the bulk density ($n = n_S/d$) [32].

2.1.5.1.3 The van der Pauw Technique

Traditionally four point probe (4PP) is considered as standard measurements tool for resistivity characterization, however this technique provides no means of decoupling the effects of mobility enhancement and carrier density increase. Van der Pauw sheet resistance measurements were used as they avoid the penetration issues associated with the 4PP technique. In a 4PP measurement, the efficacy of the probe contacts is assured by weighting the probe arm. This results in penetration of the probe tips into the sample. As a result of the ultra-shallow nature of the implant profiles being investigated, this penetration can result in large errors in the measured sheet resistances. Van der Pauw measurements proceed through deposited ohmic contacts rather than weighted mechanical contacts, thus avoiding these errors.

So in order to determine both the mobility, μ and the sheet density, n_s a combination of a resistivity measurement and Hall measurement is needed. The Van der Pauw technique, due to its convenience, is widely used in the semiconductor industry to determine the resistivity of uniform samples. The objective of the resistivity measurement is to determine the sheet resistance, R_S. Van der Pauw demonstrated that there are actually two characteristic resistances R_A and R_B, associated with the corresponding terminals shown in figure 2.5 R_A and R_B are related to the sheet resistance, R_S through the Van der Pauw equation [33]. The bulk electrical resistivity ρ can be calculated as in equation 2.6:-

$$\rho = R_S d. \qquad (2.6)$$

The objective of the Hall measurement in the Van der Pauw technique is to determine the sheet carrier density, n_s by measuring the Hall voltage, V_H. The Hall voltage measurement consists of a series of voltage measurements with a constant current, I and a constant magnetic field, B applied perpendicular to the plane of the sample. Once the Hall voltage V_H is acquired, the sheet carrier density, n_s can be calculated via $n_s = IB/q|V_H|$ from the known values of I, B, and q [34].

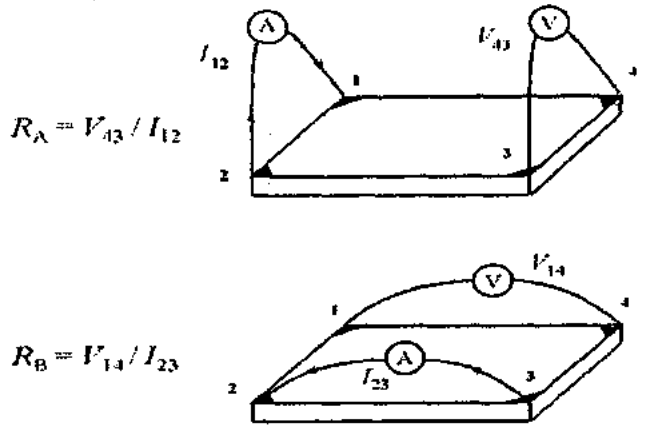


Figure 2.5: Schematic of the Van der Pauw configuration used in the determination of the two characteristic resistances R_A and R_B.

2.1.5.2 Semiconductor Characterization System Keithley Model 4200

Electrical characterization is important in determining how much the junction is efficient and behaves in different annealing regime. Keithley Model 4200-SCS Semiconductor Characterization System is able to simply test and analyze critical electrical measurements [34]. The Model 4200-SCS is well-suited for performing a wide range of measurements, including DC and pulsed current-voltage (I-V), capacitance-voltage (C-V) and capacitance-frequency (C-f) because it is an integrated system that includes instruments for making DC and ultra-fast I-V and C-V measurements, as well as control software, graphics, and mathematical analysis. Keithley's Model 4200-CVU instrument comes as a module that plugs into any available instrument slot of the Model 4200-SCS Semiconductor Characterization System, allowing fast and easy capacitance measurements from femto-Farads to nano-Farads, at frequencies from 10 kHz to 10 MHz. Developed with the most modern and high performance circuitry available, the Model 4200-CVU design provides intuitive point-and-click setup, simple cabling, and built-in element models that eliminate the guesswork in obtaining valid C-V measurements. Good for advanced CMOS pulse I-V testing and high speed single pulse charge trapping [35].

2.1.5.3 CV System

Electrical measurements have also been performed on a Material Development Corporation (MDC) Probe Station equipped with a Keithley 237 voltage source/picoammeter and an Agilent 4980A precision LCR meter. This set-up is computer controlled by the MDC software package CSM/Win Quiet CHUCK. The CV plotting system is customized with the above mentioned MDC mercury probe, hot-chuck and with a capacitance–voltage meter that performs measurements using a low frequency measurement method as shown in figure 4.4. The CV-plotting system includes components such as an output device, memory (random access memory, read only memory, a hard disk drive), and a processor or CPU. The processor is in communication with the memory, capacitance–voltage meter and out-put device. Any desired output devices can be employed in the CV plotting system (printer, digital plotters and network devices) to report, store, graph or transfer the measurement data. The capacitance voltage meter has two electrodes or terminals for connection to a probe, a force electrode or terminal and a sense electrode or terminal. These electrodes are connected to a probe station which acts on a semiconductor wafer to obtain electrical measurements. One of the electrodes is connected to an area that is much larger than the area of the mercury tip and faces semiconductor wafer. Then capacitance voltage measurement is taken by using low frequency measurement method and quasi static measurement method. In this work MDC /CSM is chosen because we can get high resolution at the probe tip (DC biasing down to millivolts and capacitance measurement down to femto-farads) and can measure Low capacitance (pico-farad and smaller values) [37, 38].

2.1.6 Ellipsometry

According to J. A. Woolam 2008 Spectroscopic Ellipsometry (SE) is unconventional but one of best non-contact, non-destructive tool to study the optical properties [39, 40]. Spectroscopic Ellipsometry (SE) is traditionally used in the Ultra–Violet, visible and near IR wavelength region (250–1850 nm) for the measurement of layer thicknesses (from sub-nanometer thickness up to tens of microns and the optical properties from transparent to absorbing materials), refractive indices and carrier concentrations [39, 41, 42].

As we know that Ellipsometry is a sensitive optical technique for determining properties of surfaces and thin films, so if linearly polarized light of a known orientation is reflected at oblique incidence from a surface then the reflected light is elliptically polarized. The shape and orientation of the ellipse depend on the angle of incidence, direction of the polarization of the incident light, and the reflection properties of the surface. We can measure the polarization of the reflected light with a quarter-wave plate followed by an analyzer; the orientations of the quarter-wave plate and the analyzer are varied until no light passes though the analyzer. From these orientations and the direction of polarization of the incident light we can calculate the relative phase change and the relative amplitude change, introduced by reflection from the surface. If the sample undergoes a change, for example a thin film on the surface changes its thickness and then its reflection properties will also change [39]. Measuring these changes in the reflection properties allow us to deduce the actual change in the film's thickness.

Thickness measurement of ultra shallow junction by Ellipsometry is also reported by different authors like Guibertoni. D. at al, 2009, reported junction depth (5.2-15.4 nm) by using Arsenic dose $1\times10^{15}cm^{-2}$ [43]. Cherroret. N. et al, 2008 noticed that the change in refractive index for as-implanted samples is due to the thermo-optic effects [44]. Lautenschlager. P. at al, 1987 measurements show that the complex dielectric function (and thus the complex refractive index) of implanted silicon differs from that of annealed silicon [45]. Bugajski. M. et al, 1985 measurements show that the increase in dielectric function is due to band gap extension. Vellie. A. et al, 2012) achieve the lowest contact resistance in sub 45 nm CMOS devices [47]. NiSi films with thickness 20–60 nm were prepared by rapid thermal annealing (temperature 230–780 °C) [48, 49].The primary application of Ellipsometry is to characterize film thickness and optical constants. It is reported that Ellipsometer is a flexible instrument and can characterize any type of thin films; dielectrics, organics, semiconductors, metals, and more. Wide spectral range and variable angle allow it to diagnose many multi-layered structures; it can collect over 700 wavelengths from the ultraviolet to the near infrared all simultaneously [39, 40, 46, 50].

2.1.7 X-Ray Diffraction

X-ray diffraction (XRD) is a versatile technique primarily used for phase identification of a crystalline materials and can provide information on chemical composition and unit cell dimensions of manufactured and natural materials. Measurement tools based on X-ray techniques (XRD, XRR, XRF) have proven to be reliable and powerful. No other technique offers the unique combination of benefits, non-destructive measurement, accuracy, precision, and absolute analysis for ex-situ investigation of epitaxial layers, heterostructures and superlattice systems [51, 52, 53].

2.1.7.1 Historical background of X-Ray Diffraction

X-Ray scattering measurements appeared as a very sensitive technique to detect damage in single crystal materials in the 1980's. In 1982, Speriosu studied the implantation of silicon ions in gallium arsenide, silicon and germanium crystals for different implant doses (Speriosu et al., 1982). This was explained a few years later by Servidori who measured damage in ion implanted silicon using X-Ray Diffraction (XRD) (Servidori, 1987) and showed how these measurements can be a powerful diagnostic technique for structural investigation in the field of ion implantation. Indeed, when ions are introduced in a crystal, interstitial type defects are generated leading to a distortion or strain of the lattice. Noda et al. describe the formation of the end of range defects to the clustering of silicon interstitials in the EOR region of the indium profile [51, 52]. XRD of In+C co-implanted Si-substrate have also been reported. X-Ray diffraction measurements calculations provide useful means for studying the strain profile of ion implanted semiconductor materials, because due to ion implantation strain arises in the substrate. However, the strain does not remains constant but varies as a function of junction depth and annealing temperature. This strain is measured by XRD [51, 53, 54].

XRD can be broadly broken down into two general processes: powder diffraction and single crystal diffraction. In the present context we concentrate on single crystal diffraction which is a non-destructive means of investigating the crystalline properties of a sample. Due to its sensitivity to inter-planar spacing in the crystal lattice,

XRD presents a means of determining a range of material characteristics investigable through measurement of this property, including sample crystallinity and strain [55, 54].

2.1.7.2 Bragg's Law

Light scattering results in diffraction, as opposed to common reflection, when the spacing between scattering centers is greater than the radiation wavelength [55]. Under this condition, superposition of scattered wave fields results in the production of interference patterns with angular dependent intensity distributions. For crystalline diffraction, the concept of lattice planes within the crystal is crucial. Within these planes, the concatenation of spherical waves, within a very short distance, reduces to a plane wave, with wave fronts parallel to, and a propagation vectors perpendicular to, the originating planes. The consideration of lattice plane scattering thus allows a great simplification of crystalline diffraction processes. In his theoretical framework, Bragg made use of this structural simplification and considered each set of lattice planes in isolation. This lead to Bragg's Law which relates the diffraction peak angle to the path length difference between beams scattered from successive lattice planes within a set [55], as shown in equation 2.7:-

$$n\lambda=2d_{hkl}\sin(\theta) \qquad (2.7)$$

Where n, is an integer associated with the order of Bragg reflection and λ, is the wavelength. Bragg's law provides a simple and intuitive means of relating experimentally observed angular peak positions with the average spacing between lattice planes of interest. For three dimensional applications however, and calculations of diffracted intensities, more elegant and powerful treatments are required. These treatments come in the form the kinematical and dynamical theories of diffraction. These theories can be shown to have the same underlying principles and differ only in their levels of approximation. As such, the more complete dynamical theory builds upon fundamentals laid out by the simpler and more intuitive kinematical theory.

From Bragg's law, it can be inferred that high levels of crystallinity are required within the sample in order to satisfy equation 2.6 for only one angle; indeed peak

broadening is indicative of crystallinity relaxation within the sample, as the Bragg condition is satisfied [56].

2.1.7.3 Kinematical Theory of X-Ray Diffraction

Kinematical theory describes the crystal under test as an amalgamation of smaller crystallites (ideally imperfect) and assumes that the diffracted intensity from each of these crystallites simply add together, i.e. regions are incoherent [52].

The result of this incoherence is that the intensity of the scattered light, when added with consideration to phase, is small with respect to the incident light. This allows both the loss of incident intensity and the interference between the incident and scattered light to be neglected. In addition to this, kinematical theory considers only a single scattering event per photon. The result of these approximations is that the theory's ability to accurately predict diffracted intensities is severely limited; the theory does however predict reasonably accurate diffraction angles and allows the expansion of Bragg's Law to 3-dimensions. The major revelation of the kinematical theory is the concept of the reciprocal lattice, which reveals the intimate relationship between the lattice periodicity and the angles of peak diffraction [54].

2.1.8 Rutherford Backscattering Spectroscopy (RBS)

Rutherford Backscattering Spectroscopy (RBS) is a powerful tool to characterize defect densities, thickness and structures in the near surface region of such thin layers [55]. It has a good depth resolution of the order of several nm, quantitative without the need for reference samples, nondestructive, and a very good sensitivity for heavy elements of the order of parts-per-million (ppm). A target is bombarded with ions at an energy in the MeV-range (typically 0.5–4 MeV), and the energy of the backscattered projectiles is recorded with an energy sensitive detector, typically a solid state detector. The analyzed depth is typically about 2 μm for incident He-ions and about 20 μm for incident protons. This technique is able to provide quantitative determination of the composition of a material and depth profiling of individual elements. RBS by the analyzing beam itself cause radiation damage but it can be minimized by carefully choosing the analyzing parameters, like total charge collection

on one analyzing spot [58]. The drawback of RBS is the low sensitivity for light elements, which often requires the combination of other nuclear based methods like nuclear reaction analysis (NRA) or elastic recoil detection analysis (ERDA). RBS includes all types of elastic ion scattering with incident ion energies in the range 500 keV to several MeV. Usually protons, 4He, and sometimes lithium ions are used as projectiles at backscattering angles of typically 150°–170°. Different angles or different projectiles are used in special cases.

2.1.8.1 Theory of Rutherford Back Scattering Spectroscopy

In 1911, Lord Ernest Rutherford first time introduced this technique. This is the most widely used technique in the semiconductor industry. In this process high energy ions (He^{+} He^{++}, H^{+}) impinge on the solid surface and elastically collide with the lattice atoms. Some of the ions are absorbed and some are backscattered into a detector, which measures the number of backscattered particles and their energy [59]. This backscattered energy of ions depends on the mass of the target material and the depth at which scattering takes place, if the mass of the target material is high, backscattered energy will be high and for low mass target material the energy will be low. Since the mid-1970s, Rutherford backscattering spectrometry (RBS) has become a mature and powerful technique for characterizing defects and composition of thin solid films [60].

It is used to measure the number and energy of ions in a beam, which backscattered after colliding with atoms in the near-surface region of a sample at which the beam has been targeted. In RBS, when the incident ions of a given energy move along the sample, losing energy during their path, and scattered by atomic collision. The backward scattered ions are detected and energy analyzed to attain the information about various facets of the sample. The interaction between a projectile ion and target atom can be explained as an elastic collision between two remote particles and expressed in terms of a scattering cross-section. The projectile energy after the collision can be linked to its energy before the collision by means of a kinematic factor. As the ion passes through the scattering medium, it undergoes a typical energy loss dE/dx. Which means the scattered ion energy not only depends on the kinematic factor but also on the depth from the sample surface where the scattering takes place. The incident ion

loses some energy to achieve this depth and after scattering, it again loses some energy to move out of the sample from that depth. Thus the energy of the detected scattered ion encloses the depth information [60].

RBS is the only surface analysis technique, which does not rely upon use of standards for quantification. The sensitivity in RBS is a function~ Z^2 and hence it is best suited for analysis of heavier elements or layers on lighter substrates. For the measurement of layer thickness and depth composition four physical phenomena of RBS are required as given below:

1. Kinematic Factor
2. Scattering Cross-section
3. Sopping Cross-section
4. Energy Straggling

2.1.9 Introduction of Grazing Incidence X-Ray Fluorescence (GIXRF)

A recently emerging technique Grazing Incidence X-Ray Fluorescence (GIXRF) in the soft X-Ray range is an alternative to SIMS is a high potential tool for analysis of thin layers. Which is non-destructive and only suitable for thin layers up to some 30 nm [61, 62, 63].

The total reflection of X-rays from solid samples with flat and smooth surfaces was first reported by Compton in 1923, which can be assumed to be the birth of specular reflectivity. Yoneda in 1963 reported the intensity modulation in the X-Ray diffuse scattering and in 1971 Yoneda and Horiuchi first time reported X-ray fluorescence radiation from particles, deposited on a smooth substrate, and excited by X-rays impinging the surface at an angle below the critical angle of total reflection. TXRF, also called grazing-incidence X-ray fluorescence (GI-XRF). It is based on gradually tilting the sample near the critical angle of total reflection, i.e. at grazing incidence. GIXRF technique whose probing depths are around 10 nm is very sensitive to near-surface layers and is therefore well suited for the depth profiling of Ultra Shallow

junctions in CMOS and is applied to evaluate the retained dose and dopant depth distribution [64, 65].

The method is non-destructive and is based on tilting the sample near the critical angle of reflection at grazing incidence [64]. The GIXRF quantitation of the elemental depth profile is based on ab-initio calculations, using the simulated X-ray Standing Wave field intensity (XSW), in which all relevant fundamental parameters are involved. The X-ray standing wave (XSW) field associated with GIXRF on flat samples is used here as a tunable sensor to obtain information about the implantation profile because the in-depth changes of the XSW intensity are dependent on the angle of incidence. This technique is very sensitive to near-surface layers and is therefore well suited for the analysis of USJ distributions [65].

2.1.10 Atomic Force Microscopy (AFM)

Atomic force microscopy (AFM) is a very high-resolution type of scanning probe microscopy, with demonstrated resolution on the order of fractions of a nanometer, more than 1000 times better than the optical diffraction limit. The first atomic force microscope (AFM) was made in 1986. It was of the dynamic type with vertical tip vibration [66, 67, 68, 69]. However, the first commercial instruments (since 1989) were static-force or contact AFMs. Shear-force AFM microscopes with horizontal tip vibration for distance control were developed in 1992. The dynamic-mode AFM found a new application with the commercialization of noncontact and tapping-mode AFM. The main advantage of AFM over rest of the microscopes resides in the AFM capability to image the topography both for conducting, semiconducting and insulating materials. To date, atomic force microscopy has had a widespread application as a characterization tool in many fields of sciences and engineering, from biology, to semiconductor industry. The extremely high spatial resolution reachable by this approach is one of its most attractive characteristics [68].

This technique is the measurement of behavior of roughness after implantation and thermal annealing, because The AFM is one of the foremost tools for imaging, measuring, and manipulating matter at the nano-scale. AFM Agilent system 2500 picoscan) has been used to image the extent of surface roughness caused due to ion

irradiation of the samples particularly with reference to the USJ formation in the area/depth of our interest.

Chapter No. 3

This chapter briefs literature review and leading achievements which are related to this work. Since many research groups have been already performed experiments, so it is beyond the scope to cover all the details comprehensively. The main objective of this thesis is to fabricate ultra-shallow junctions (USJs) for the application in the future generation CMOS devices by using appropriate implantation energy and dopant concentration. Therefore, it will be necessary to start with a description of the architecture of CMOS devices.

3.1 History of CMOS

In 1824 John Jacob Berzelius first isolate and identifies silicon and in 1833 Michael Faraday discovers that electrical Resistivity decreases as temperature increases in silver sulfide. This was the first investigation of a semiconductor. In 1927 Arnold Sommerfield and Felix Bloch apply quantum mechanics to solids. This allows scientists to explain the conduction of electricity in semiconductors and Liandrat first proposed in 1935 that the conductivity of a surface region in a semiconductor could be modulated by the application of a perpendicular electric field [36]. This is known as "field effect" concept. In December 1947, three researchers from Bell Labs: J. Bardeen, W. Brattain, and W. Shockley, developed point contact transistors based on field effect theory [70, 71] .It was one of the most important invention in the field of modern physical sciences. In 1939 p-type and n-type semiconductors are discovered in silicon at Bell Labs. In 1947 Shockley, Bardeen and Brattain demonstrate first point contact transistor [72]. This invention enabled transistors to replace already used vacuum tubes. In 1950 William Shockley's lab demonstrates first junction transistor. Since late 1950's the discovery and invention of new electronic semiconductor materials and the drastic reduction in the size of electronic devices has moved at a rapid pace. In 1953 General Electric Company creates the uni-junction transistor and in 1954 Texas Instruments puts silicon transistors into production [73] and at the same instant C. A. Lee at Bell Labs makes first diffused-base germanium mesa transistor with a cutoff frequency of 500 MHz as shown in figure 3.1. As a result the speed of electronic devices (particularly

integrated circuit) has grown exponentially over the same time period. Great strides have been made by companies 'such as Bell Laboratories, Intel, Westron Electric, American Telephone and Telegraph, Motorola, Rockwell, and IBM [72].

In 1955 IBM begins marketing its first transistorized computer, model 7090. In 1956 William Shockley invents the PNPN diode (Shockley diode, two of which, when packaged as a parallel pair connected in opposite directions are known as a DIAC [73]. 1958 Fairchild Camera and Instrument Corp. market their first silicon diffusion mesa transistors to RCA. 1958 Jack Kilby at Texas Instruments demonstrates the first working integrated circuit in the laboratory on September 12th [70, 71, 72]. This invention showed the world that it is possible to integrate many devices in a single chip and enhance functionality.

In 1959 Texas Instruments and Fairchild Camera and Instrument Corp. independently develop the first commercial integrated circuits- Fairchild's version demonstrating the first with planar metallised interconnection. 1963 CMOS logic circuit principles disclosed for the first time in U.S. patent 3,356,858 by Frank Wanlass of Fairchild Semiconductor. 1964 Transistor-Transistor Logic introduced by Texas Instruments and 1965 Gordon Moore discovers Moore's Law: The number of components on the most complex integrated circuit chip would double each year [74]. Since 1960 MOS transistor dimensions have been shrinking 30% every year, and recently scaling also accelerated.

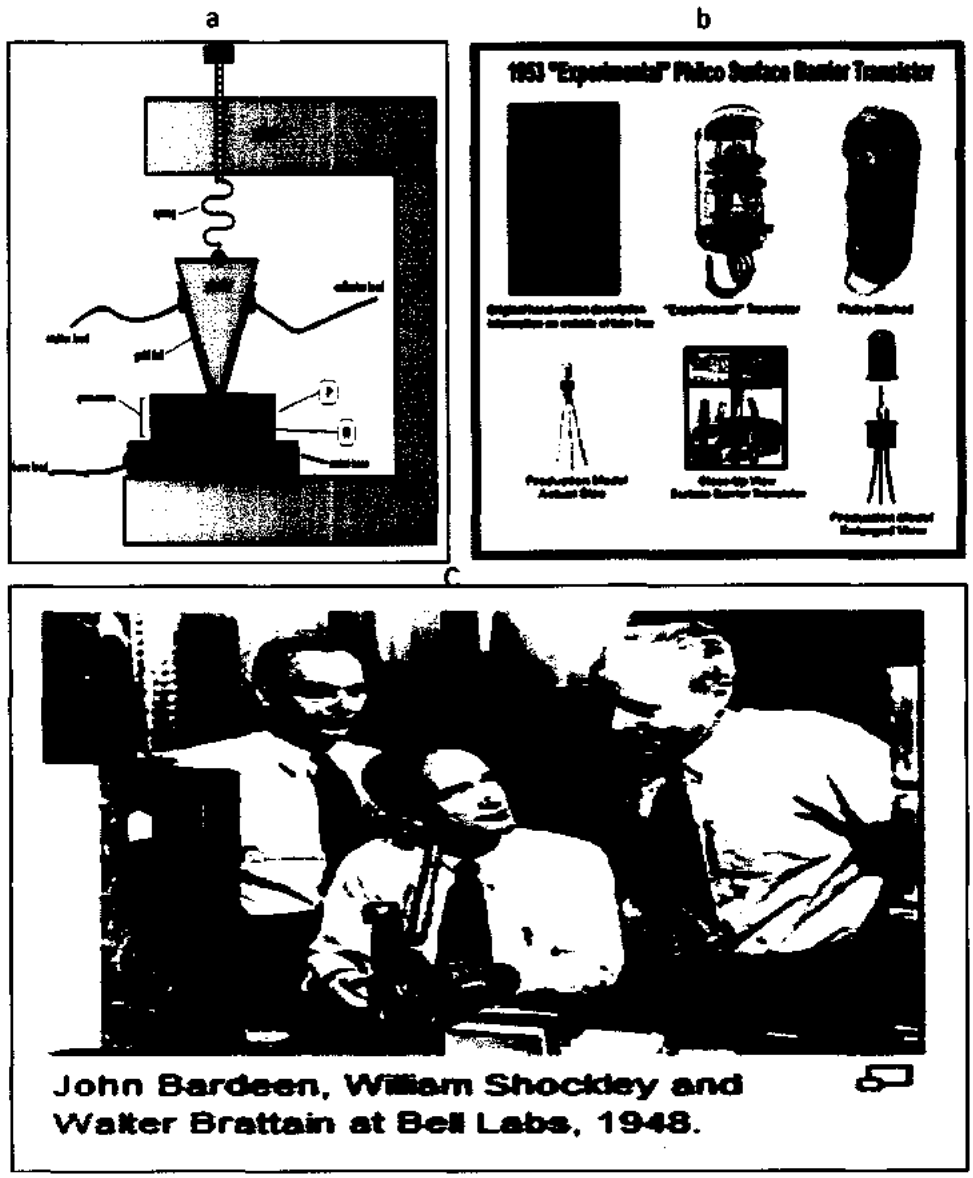


Figure 3.1: (a) An early model of a transistor. (b) Experimental Philco surface barrier transistor.(C) First point contact transistor introduced in Bell Labs [42,43,44,45].

In 1968 RCA introduces their CD4000 series CMOS logic family, which they called "COS/MOS. In 1971 Intel introduces the 4004 4-bit microprocessor, containing 2300 transistors, and considered to be the world's first single chip microprocessor. It was used on the Pioneer 10 spacecraft in 1972. 1975 Moore's Law slows, towards a doubling at present time about every 2 years [75]. 1975 IBM introduces their first "Personal Computer", the IBM 5100, which is considered to be the first portable PC (but not the first PC, which is attributed to the Altair 8800 kit launched by Ed Roberts in January 1975) based on large-scale integration (LSI) [75]. In 1977 it became clear

that in order to compete with the Japanese semiconductor markets, U.S. manufacturers would have to work together and the Semiconductor Industry Association (SIA) was created. By 1978, when Toshiaki Masuhara of Hitachi described a high-speed RAM at ISSCC, the combination of smaller lithography with the silicon-gate process enabled CMOS to compete in performance with bipolar and conventional MOS. As designers took advantage of scaling) to pack hundreds of thousands of transistors onto a chip, CMOS provided the best solution to manage the resulting power density issues. In 1980 power consumption becomes a major issue, so CMOS processes are widely adopted [76].

The SIA would later go on to create the Semiconductor Research Corporation (SRC) and Sematech. In addition, in 1992, the SIA introduced its first 15-year National Technology Roadmap for Semiconductors. The purpose of the roadmap was to outline semiconductor research needs so that future challenges could be overcome. The roadmap has been revised several times and in 2000 became the International Technology Roadmap for Semiconductors (ITRS) [77]. Today, Ultra Large Scale Integration (ULSI) is in use and it is referred for 100,000 and more than 100,000 transistor on a single chip [78]. Today feature size are down to about 4 nanometer (nm) and research is continuing on reducing feature size even more. At the present rate of development of the integrated circuit (IC) industry, the feature sizes keep reducing at an average rate of 11% per year [79]. The Pentium 4 MP manufactured by Intel with minimum specification of 3.6 GHz manufactured on 65nm process approximately has 230 million transistors in it [80].

Scaling, which was first stated by Gordon Moore in 1965, as Moore's law becomes the basis of continual downscaling progress of CMOS, this scaling methodology has worked very well for several decades up to micro regime but when Si CMOS technology enters into nano-regime some functional and practical limitations hinder the traditional scaling of transistors.

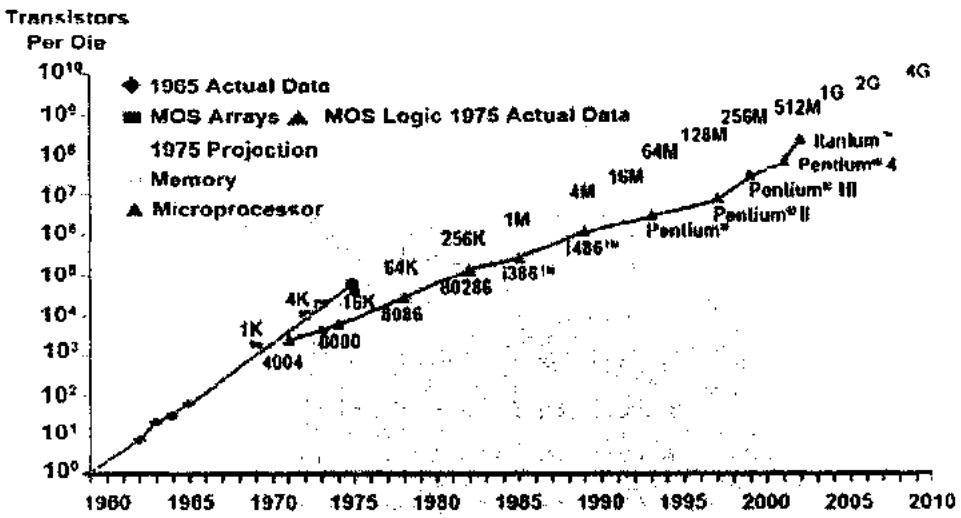


Figure 3.2: Moore's law of scaling. The number of transistors on a chip has been exponentially [74].

Moore's Law also means decreasing costs. As silicon-based components and platform ingredients gain in performance, they become exponentially cheaper to produce, and therefore more plentiful, more powerful and more seamlessly integrated into our daily lives (Intel Website). Up-gradation of this law due to advancement of technology gives rise to such a detail that as shown in figure 3.3. Moore's Law till now has strictly affected history of Semiconductor Industry, but now we are facing such a problems that the parameters described by this law have about to reach its limits. The research industry is leading the commercial industry by around five years. It is not always possible to have a device commercially available that has been fabricated in the research level due to some financial limitation or non-abundance of materials related to it. So one needs to do continuous research to come up with methods to improve the feature dimensions and control the processes involved in this regard. For the level of complexity involved in the manufacturing of integrated circuits today, one needs to use both experimental and computer analysis (simulation) to have insight into the physical mechanisms involved and to analyze the effect of a particular process change or modification. This definitely makes the semiconductor industry more viable. Thus the concept of virtual fabrication earlier and modeling nowadays comes into being [79, 81].

Among the various challenges in the ITRS roadmap, scaling down the dimension of transistors is one avenue to achieve faster devices with higher functionality while creating more densely pack circuits. However, the aggressive down scaling progress has aggravated the short channel effect. To resolve the SCE, formation of ultra-shallow junctions (USJs) in the S/D region, or more particularly the S/D extension, has been identified as one of the main road blocks for device downscaling. Ever decreasing junction depth (Xj) and highly activated low sheet resistance (Rs) junctions in S/D extension junctions are desired to sustain the scaling proportion of whole device. Unfortunately, the anomalous behaviors associated with the doping processes, such as transient enhanced diffusion (TED) and dopant clustering/de-activation hinder the junction specifications required in the advanced devices [82, 83, 84, 85]. Down scaling progress of junction depth and sheet resistance is given in table 3.1, 3.2, and figures 3.3 and 3.4.

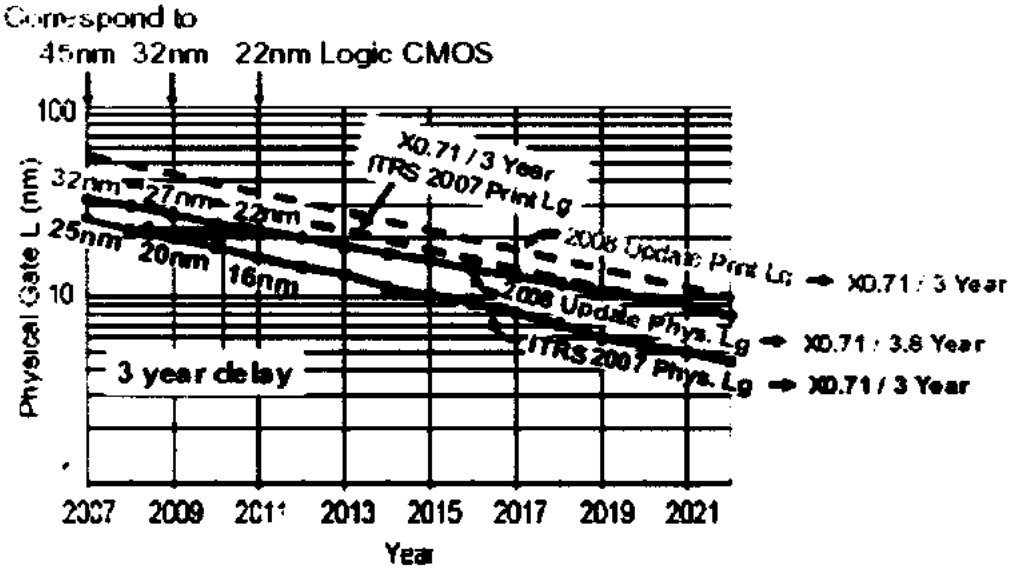


Figure 3.3: This graph shows year by year gate length reduction according to ITRS roadmap [78].

According to International Technology Roadmap for Semiconductors (ITRS) 2005 edition, Xj was ~0.36 Lg. While it modifies by introduction of high k/metal gate and offset spacers has relaxed this requirement and modifies it to be ~0.50 Lg in ITRS

2007 edition for 45nm nod and CMOS generations 32nm and beyond have source/drain extensions becomes few nm deep, 2007 road map becomes industry scale in 2016.

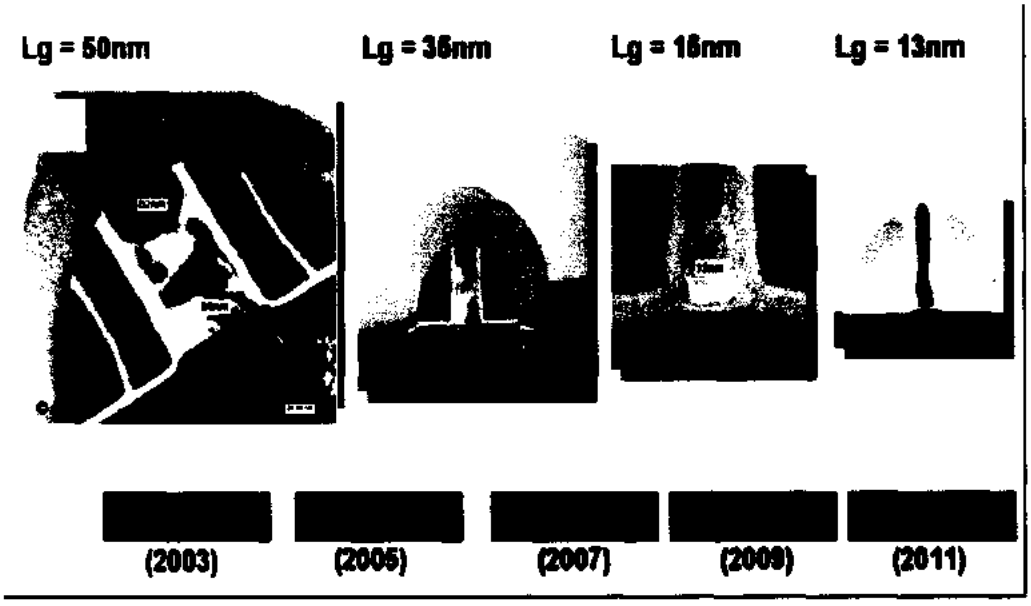


Figure 3.4: Developmental stages of transistor [83].

3.2 Trends in Ultra Shallow Junction (USJ) devices

A comparison for the formation of USJ and its related parameters with different dopants in silicon are shown in table 3.1 below.

Table 3.1: Review of parameters related to USJ for boron in silicon

Substrate Type	Energy (kev)	Dose (ions/cm^2)	Annealed temperature & time (°C/mins or s)	Sheet Resistance (ohm/sq.)	Junction Depth (nm)	References
n-type Si(100) BF2	1keV	1 x 10^{15}	Micro Wave Annealing 570°C/ 3500W	4000		86
p-type Si(100) As	1keV	1 x 10^{15}	Micro Wave Annealing 570°C/ 2800W	2000		87
N-Si B			900/10min Furnace annealed	135	55.2	88
N-Si B			950/10min Furnace annealed	116	148.6	88
N-Si B			900/10 sec Rapid Thermal Annealed	155	3.5	88

N-Si B			950/10 sec Rapid Thermal Annealed	152	9.3	88
Al	1	1×10^{16}	1		4	89
Ge		5×10^{14}	Flash anneling	1000	15	90
Si B	0.5	3×10^{15}	Un-annealed	550	13	91
PAI in Si	0.5	5×10^{14}	900/1 sec	1540	57	92
Si As	3	1×10^{15}		6	5	93
P-Si B			Un-annealed	516	30	94
Si(100) As	10	1×10^{16}	Un-annealed		13	95
n-Si B	1	1×10^{15}	Flash lamp annealing	300	24	96
N doped Silicon	15	8×10^{15}	Pre-annealed at 900/20mins	--	80	97
n-type Silicon	20	$5x\ 10^{13}$	1050//10s	1740	220	98
n-type Silicon	20	$5x\ 10^{13}$	550/60 followed by 1050/10s	1930	182	98
10 keV Ge PAI *n*-type Si	0.5	2×10^{15}	--	548	39	99
n-type Silicon	40	25×10^{13}	1050/10s	1640	222	99
n-type Silicon	0.5	2×10^{15}	800/1min	1500	140	12
n-type Silicon	40	$2.5x\ 10^{13}$	550/60m followed by 1050/10s	1760	171	99
n-Si In+C	70 13.5	5.75×10^{14} 2.22×10^{15}	1000°C /60min		40	12
-type Silicon	40	$2.5x\ 10^{13}$	550/60m followed by 1050/10s	1760	--	99
Si BF2	0.2				9.5	19
n-type Silicon	60	1.67×10^{13}	as-implanted	--	184	99
n-type Silicon	60	1.67×10^{13}	1050/10s	2350	180	99
n-type Silicon	60	1.67×10^{13}	550/60m followed by 1050/10s	1960	--	19
n-type Silicon	77	$1.25x\ 10^{13}$	as-implanted	--	146	19
n-type Silicon	77	$1.25x\ 10^{13}$	1050/10s	3780	152	19
n-type Silicon	77	$1.25x\ 10^{13}$	550/60m followed by 1050/10s	3520	--	19
n-type Silicon	5	2×10^{14}	1100/30s	--	35	100

30keV Ge PAI n-type Si	0.5	1×10^{15}	700/5s	443	32	101
30 keV Ge PAI in Si	1	1×10^{15}	1300	500	20	102
8E14 Si PAI in Silicon	0.5	5×10^{14}	900/1s	1540	57	103
Lowly doped n-type Si	20	1×10^{14}		1050	85	104
slowly doped n-type Si	20	1×10^{15}		230	44.7	104
P-Si In	115	1×10^{14}	Spike annealing 1050°C		24	104
P-Si As	2	1.5×10^{15}	Spike annealing 1050°C			104
Sb doped Silicon	--	5.7×10^{14}	800/10mins	625	38	105
Silicon Substrate	0.5	1×10^{15}	FLA 1100/20ms	1200	50	106
Silicon Substrate	0.5	1×10^{15}	FLA 1200/20ms	780	55	106
Silicon Substrate	0.5	1×10^{15}	RTA 1100/1s	800	68	106
Silicon Substrate	0.5	1×10^{15}	RTA 1200/1s	625	81	106
Silicon substrate	0.8	1.2×10^{15}	1075/s	1130	27	107
Silicon substrate	0.5	1.2×10^{15}	1075/s	1500	--	107
Silicon substrate	80	1×10^{15}	1100/10s	100	26	108
Silicon Substrate	1	1×10^{15}	910/220s	580	37	15
n-Si In+C	70 13.5	5.8×10^{14} 5.57×10^{14}	650/60min		34	12
c-Silicon substrate	0.5	2×10^{14}	Arc lamp spike Anneal at 1150	550	45	27

Chapter No. 4

This chapter gives a description of the entire experimental details used to obtain the data and sample strategies. Procedures from the initial sample processing (simulation) to physical and electrical characterization techniques used in this work are also briefly elaborated

4.1 Simulation Techniques

We performed rigorous simulations on four sets of samples In+C co-implanted (p-type silicon), In+C co-implanted (n-type silicon) In+B implanted (n-type silicon), and boron implanted (n-type silicon) with various ion energies at different incident angles using Stopping and Range of Ions in Matter (SRIM) code in order to find out the resultant range and damage profile in the Si due to Indium + Carbon ions and boron ions. Further, Silvaco TCAD code was used to predict the distribution of defects in the Si substrate due to the carefully chosen ion implant schedules.

4.1.1 Stopping and Range of Ions in Matter (SRIM)

An international simulation packages (computer codes), namely industrially trade-off IBM`s Stopping & Range of Ion in Matter (SRIM)" introduced by Ziegler. J. F, 2008 have been used in this work [104]. In this package different input parameters like energy, angle, substrate and implantation species have been set in order to achieve required doping profile. In general by changing the value of each input parameter such as energy, fluence (dose) and angle of incidence of the incident beam simulation were achieved showing various output parameters of the implantation which are steady state broadening, sputtering yield, nuclear and electrical energy deposited, mean range and standard deviation.

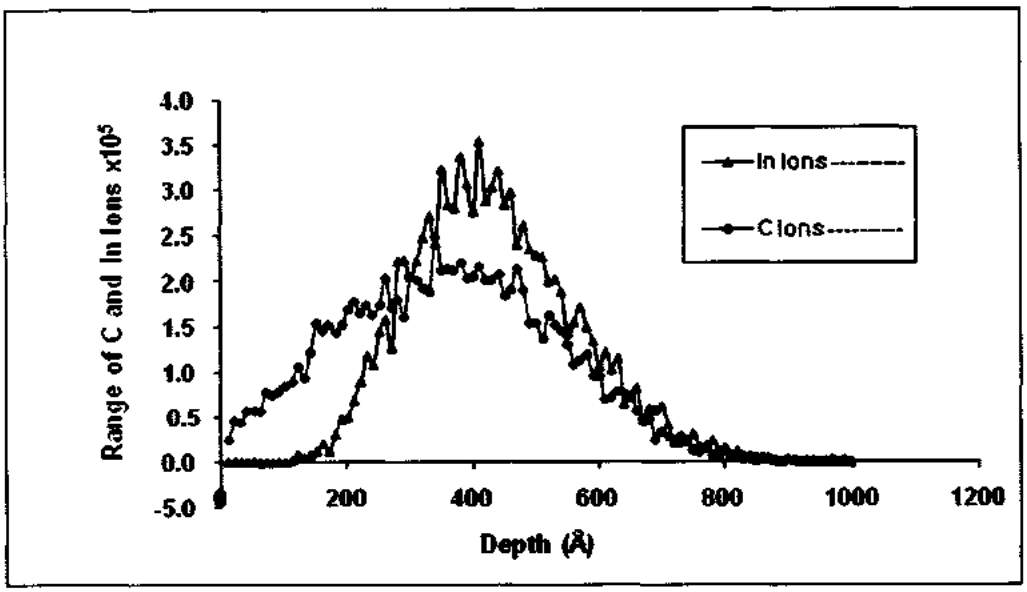


Figure 4.1: Results of SRIM simulation showing range of indium and carbon in silicon.

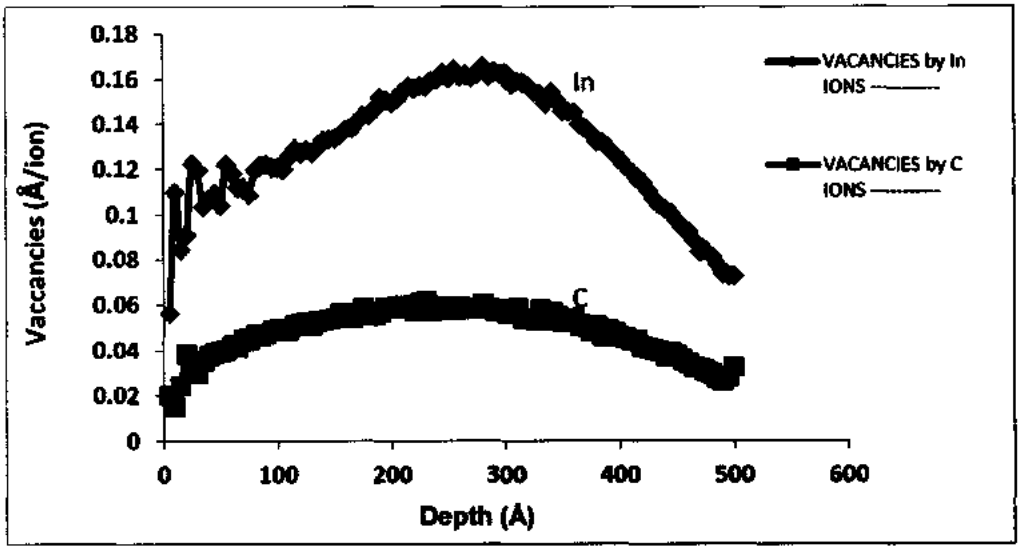


Figure 4.2: Results of SRIM simulation showing defects generated in silicon due to indium and carbon implantation.

By using SRIM 2008, the output parameters are collision plots in the form of longitudinal and lateral directions, ion distribution, lateral distribution, ionization, phonons, energy to recoil and vacancy requirements such as specified depth attained by dopant ions for ultra shallow junction and implantation energy for minimal damage

event created by ion beams of indium, carbon and boron on silicon substrate were measured. Some output parameters are shown in figures 4.1 and 4.2.

4.1.2 Technology computer-aided design (TCAD)

Simulator for Technology Computer-aided Design (TCAD) has become a fundamental tool in silicon industry for the fabrication of silicon based devices [9]. This TCAD tool package is made up of four modules: Senturus Devices, Senturus Process, Senturus Editor, and workbench. It is designed for electronics with a recently developed optoelectronics module, capable of fully coupled electro-opto-thermal 3D modeling with mature and accurate numerical computation. Besides its high accuracy, Senturus also provides many advantages such as an advanced carrier tunneling model to monitor non-local tunneling, thermionic emission and direct tunneling, fast and accurate simulation of all critical fabrication steps used in CMOS and power device technologies and accurately predicts multi-layer topology, dopant distributions, and stresses in various device structures. In this research TCAD is chosen as process simulator because ATHENA provides a convenient platform for simulating processes used in semiconductor industry: ion implantation, diffusion, oxidation, physical etching, deposition, lithography, stress formation and silicidation [10]. With the scaling down of device size, ultra shallow junction technology becomes more and more important for the suppression of short channel effects, resulting in the requirement of lower energy ion implantation. Shallow junction formation requires a lower energy ion implantation, lower annealing temperature, and shorter annealing time, because in boron TED (Transient Enhanced Diffusion), occur during high-temperature annealing. Therefore, there is an urgent need to simulate defects in TCAD [5].

The modeling and simulation of disorder induced by duly damaged of In^+, C^+ and Si^+ done with the help of SILVACO TCAD-trade-off industrial solution. Simulation of devices with given experimental conditions are shown in figure 4.3. The p- type and n-type Si (100) substrate manufactured by Czochralski *(CZ)* Growth Method are used as starting wafers in this study. By using suitable choice of implantation parameters, it becomes possible to obtain continuously variable material properties from crystalline to amorphous structure, because ion implantation caused

damage formation, which changes the optical and electronic properties of a semiconductor.

Pre-amorphization will occur by the implantation of Si^+ ion with dose 5×10^{15} ions/cm^2 and implant energy of 0.5 keV. The n-type and p-type Si substrates then implanted with indium ions at an energy of 70 keV at room temperature using fluence ranging from 5.7×10^{14} ions/cm^2 with 7 degree tilt and 24 degree twist angles and then carbon is co-implanted at room temperature with energy 10 keV C^+ ions using fluence 3.4×10^{15} ions/cm^2 at 8 degree tilt and 22 degree twist angles as shown in Table 4.1. The sample then subsequently annealed ranging from 600 to 1100°C in N_2 atmosphere for 60s in order to analyze their structural recovery. Than the impact of heat treatment on the profiles was achieved, it will be discussed in chapter. 5. Damage introduction during ion irradiation and its removal during a thermal annealing step are the main key issues to emphasize in order to analyze their structure.

4.2 Experimental Ion Implantation

Commercially grown, CZ p-type and n-type Si wafers of orientation (100) with initial resistivity between 4-7 Ω/square were taken to process with pre- designed implant recipes. They were at first implanted with Si at an energy of 500 eV and a fluence of $\phi^{Si}\approx5\times10^{15}$ at/cm^2 in order to achieve an amorphous layer of approximately 1μm thickness in accordance with the above mentioned simulations. Pre-amorphization implants were carried out to enhance the degree of electrical activation in the samples.

Wafers were then implanted with 5.7×10^{14} ions cm^{-2} Indium atom with 8° tilt and 24° twist at 70 keV energy. This was followed by Carbon atoms co-implanted at the same angles with an energy of 10 keV at a fluence of 2.5×10^{15}, 3.0×10^{15}, 3.2×10^{15}, 3.4×10^{15}, and 3.6×10^{15} ions cm^{-2}. The best recipe with Indium dose of 5.7×10^{14}, ions cm^{-2} chosen for getting ultra shallow junction below 65 nm node is given in Table 4.1.

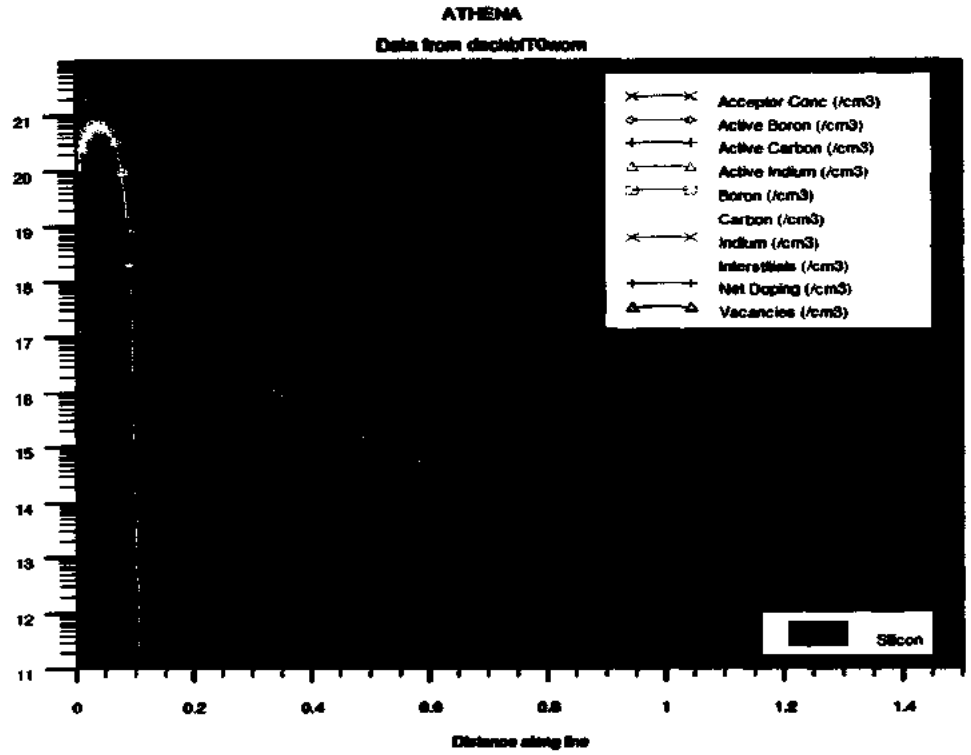


Figure 4.3: Damage distribution, resulting from a 70 keV indium implantation and 10 keV carbon co-implantation in silicon. Along X-axis the depth is in micron and along Y-axis defects are in log scale.

By using this recipe, hundreds of samples were prepared by In+C co-implanted silicon substrate as shown in Table 4.1. Electrical characterization shows that formation of junction occurs in 40 samples, which were selected for further processing. In second set of experiment commercially, CZ grown n-type Si wafers of (100) orientation were processed according to pre-designed implant recipes. Wafers were then implanted with 1×10^{15} boron at/cm^2 at 8° tilt and 24° twist having 30 keV energy. The processed wafers were then diced into squares of 1cm^2 sizes and subsequently subjected to Rapid Thermal Annealing (RTA) between 600 and 800°C for 60 sec dwell and carefully designed ramp-up time as shown in Table 4.2. The higher annealing temperature (between 800 to 1100°C) are purposely not chosen for the specific study to focus on the defect-doping matrix influencing the formation of ultra shallow junction on the desired implantation strategy with relatively low thermal budget. All the implants have been performed at commercial accelerator facility, whereas the activation-annealing experiments were performed in Berkeley National Laboratory.

4.2.1 Ion-Implanter

An ion implanter consists of in source, ion accelerator and ion focusing arrangements. The ion sources produce either positive or negative ions from neutral atoms of elements. These ions are initially formed by stripping electrons from source atoms in plasma and then extracted and passes through a mass-analyzing magnet, which selects only ions of a desired species, isotope, and charge state as shown in figure 4.4. The beam of ions is then accelerated using a potential gradient column, with energy ranging from 10-200 keV (indium at 70 keV, carbon at 10 keV and boron at 30 keV). A series of electrostatic and magnetic lens elements confine and shape the resulting ion beam and transferred these energetic ions to the initially stationary target. Energetic recoil Si atoms produced by collisions with the incoming dopant ions will also collide with other Si atoms and if sufficient energy is transferred they in turn will be displaced. This process continues resulting in a collision cascade. The collision cascade produced by single heavy implanted ions, such as In, As, Sb, and Xe, tends to produce small amorphous zones. After a series of collisions with different target atoms an ion will come to rest at some range within the Si once it has lost all its energy. For a given implant species the lower the implant energy, the shorter the range will be. The statistical nature of the slowing down process produces a distribution of the implanted ions within the Si about some mean depth. The implanted ion distribution is approximately a Gaussian distribution [105]. When a certain implant concentration has been exceeded these zones will spatially overlap forming a continuous amorphous layer. Implanted light ions such as B create less damage to the Si lattice, but damage will build up until a certain critical concentration of defects exists when the crystal structure can collapse into an amorphous structure. It is difficult to produce an amorphous layer with light ions and will require substantially higher implant doses to achieve compared to heavy ions [106].

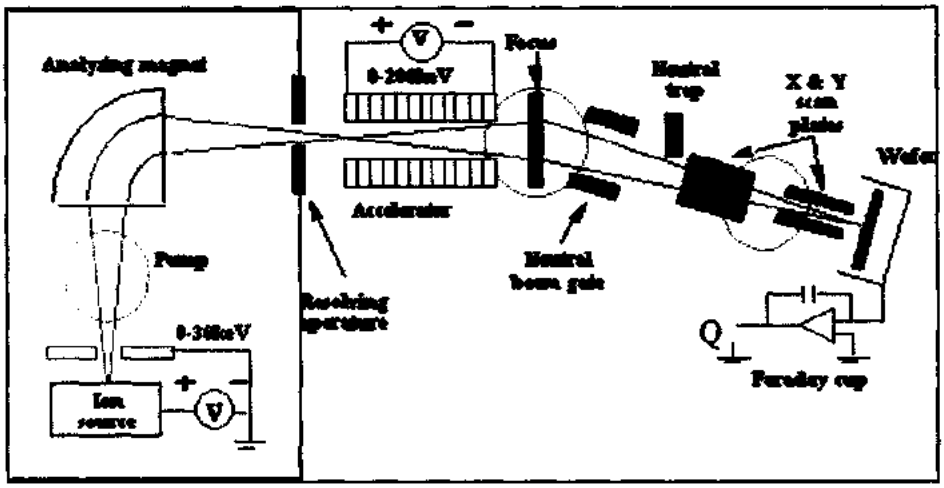


Figure 4.4: A typical Ion implanter.

4.3 Annealing Techniques

After the formation of the desired junction, the samples were subsequently subjected to Rapid Thermal Processing (RTP) anneals at temperatures 600,650,700,750 and 800°C for 60 sec, because rapid thermal annealing is proven to be a successful method for producing junction depths according to the scaling of CMOS technology roadmap with its ability to give spike annealing and to improve activation and diffusion of dopants.

4.3.1 Rapid Thermal Annealing (RTA) and Furnace Annealing Techniques

After ion implantation the samples were annealed by RTA (600-800°C) for 60 sec and furnace annealing 1050°C for 15 min. Fast ramp up and ramp down rates were used. The goal of the post implant annealing is to restore the silicon lattice to the pre-implant state and to electrically activate the implanted dopant atoms. Since most implanted dopants do not occupy substitutional sites upon implantation a thermal step is required to provide the energy required to move the atoms to the correct lattice site. Electrical activation of the dopants in an amorphous layer proceeds differently from the activation of dopants within primary crystalline damage.

Electrical activation in amorphous layer occurs as the impurities are incorporated into lattice sites during recrystallization. Electrical activation in areas of primary crystalline damage proceeds with more complexity. The movement of doping atoms according to a dopant gradient in a semiconductor material is called diffusion, which occur during high temperature processing steps, either as intentional or as parasitic effect. Due to the requirement of very shallow junction in modern semiconductor technology, diffusion is mainly a parasitic effect of the annealing step after ion implantation or of an oxidation step which is performed at high temperatures [21].

The time and temperature variations of the heat treatment of implanted samples is known as the annealing cycle, which has a significant influence on the sitting of implanted impurities within the host substrate lattice. It is the installation of impurities within the host lattice, which determine the resistivity and consequently the conduction properties of the material. The concentration of activated impurity atoms is a function of the implanted dose as well as the annealing cycle. The details of Samples processing for In+C co-implanted p-type, In+C co-implanted n-type Si and B implanted n-type silicon are given in Table 4.1.and 4.2.

Table 4.1: Breakdown of In+C co-implanted Si samples.

S. No	Wafer ID	Sample ID	Dose and implantation energy (Si for PA)	Dose and implantation energy (In)	Dose and implantation energy (C)	Annealing (C) Temp/time
1	Si (100) n-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	650/60sec furnace annealed
2	Si (100) n-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	Un-annealed
3	Si (100) n-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	Un-annealed

4	Si (100) n-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	800/60sec RTA
6	Si (100) n-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	650/60sec RTA
7	Si (100) n-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	700/60sec furnace annealed
8	Si (100) n-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	700/60sec RTA
9	Si (100) n-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	750/60sec RTA
10	Si (100) p-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	650/60sec furnace annealed
11	Si (100) p-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	Un-annealed
12	Si (100) p-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	Un-annealed
13	Si (100) p-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	Un-annealed

14	Si (100) p-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	650/60sec RTA
15	Si (100) p-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 KeV	3.4×10^{15} Atoms/cm^3 10 KeV	700/60sec furnace annealed
16	Si (100) p-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	700/60sec RTA
17	Si (100) p-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	750/60sec RTA
18	Si (100) p-type	In +C co-implanted	5×10^{15} Atoms/cm^3 500 eV	5.7×10^{14} Atoms/cm^3 70 keV	3.4×10^{15} Atoms/cm^3 10 keV	800/60sec RTA

Table 4.2: Breakdown of B implanted n-type Si substrate.

Sample. No	Sample ID	Dose and implantation energy of Boron	Annealing Temperature (°C)
1	S#1	1×10^{15} Atoms/cm^3 30 keV	As-implanted
2	S#2	1×10^{15} Atoms/cm^3 30 keV	As-implanted
3	S#3	1×10^{15} Atoms/cm^3 30keV	As-implanted
4	S#4	1×10^{15} Atoms/cm^3 30 keV	As-implanted
5	S#5	1×10^{15} Atoms/cm^3 30 keV	As-implanted
6	S#6	1×10^{15} Atoms/cm^3 30 keV	As-implanted
7	S#7	1×10^{15} Atoms/cm^3 30KeV	As-implanted
8	S#8	1×10^{15} Atoms/cm^3 30 keV	As-implanted
9	S#9	1×10^{15} Atoms/cm^3 30 keV	As-implanted
10	S#10	1×10^{15} Atoms/cm^3 30 keV	As-implanted

11	S#11	1×10^{15} Atoms/cm^3 30keV	As-implanted
12	S#12	1×10^{15} Atoms/cm^3 30 keV	As-implanted
13	S#13	1×10^{15} Atoms/cm^3 30 keV	As-implanted
14	S#14	1×10^{15} Atoms/cm^3 30 keV	As-implanted
15	S#15	1×10^{15} Atoms/cm^3 30KeV	As-implanted
16	S#16	1×10^{15} Atoms/cm^3 30 keV	As-implanted
17	S#17	1×10^{15} Atoms/cm^3 30 keV	As-implanted
18	S#18	1×10^{15} Atoms/cm^3 30 keV	As-implanted
19	S#19	1×10^{15} Atoms/cm^3 30keV	As-implanted
20	S#1	1×10^{15} Atoms/cm^3 30 keV	600/60sec RTA
21	S#1	1×10^{15} Atoms/cm^3 30 keV	700/60sec RTA
22	S#1	1×10^{15} Atoms/cm^3 30 keV	750/60sec RTA
23	S#1	1×10^{15} Atoms/cm^3 30KeV	800/60sec RTA
24	S#1	1×10^{15} Atoms/cm^3 30 keV	1050/15min Furnace annealed
25	S#9	1×10^{15} Atoms/cm^3 30 keV	600/60sec RTA
26	S#9	1×10^{15} Atoms/cm^3 30 keV	700/60sec RTA
27	S#9	1×10^{15} Atoms/cm^3 30 keV	750/60sec RTA
28	S#9	1×10^{15} Atoms/cm^3 30keV	800/60sec RTA
29	S#9	1×10^{15} Atoms/cm^3 30 keV	1050/15min Furnace annealed
30	S#14	1×10^{15} Atoms/cm^3 30 keV	600/60sec RTA
31	S#14	1×10^{15} Atoms/cm^3 30 keV	700/60sec RTA
32	S#14	1×10^{15} Atoms/cm^3 30KeV	750/60sec RTA
33	S#14	1×10^{15} Atoms/cm^3 30 keV	800/60sec RTA
34	S#14	1×10^{15} Atoms/cm^3 30 keV	1050/15min Furnace annealed

After the formation of junction we employed Keithley 4200 I-V System (especially tailored for reliable nano-regime measurements), MDC CSM CV system and Ecopia HMS 3000 Hall Measurement System to determine the sheet carrier

concentration, mobility and resistivity of these devices to improve the tolerance and reliability of data. Van der Pauw method was employed instead of the commercial four point probe, due to the shallowness of the junction and Au+Ge+Ag contacts were deposited on the surface through sintering process. After these electrical characterizations junction depth was also measured and verified by different techniques like Ellipsometry, Rutherford back Scattering (RBS), X-Ray Diffraction and Atomic Force Microscopy (AFM).

4.4 Electrical Characterization Techniques

Although the major thrust of this thesis is not in the electrical characterization of the samples, but an investigation of $^{115}In+C$ co-implanted Si would be incomplete without consideration of the impacts junction formation on the material's electrical properties of implanted species. The electrical data pertaining to this work has been published [33]. In this work, the electrical characterization was carried out using a combination of Van der Pauw (sheet resistance) and Hall Effect (carrier density) measurements, Keithley System 4200 and CV measurement System. The measurements reported in this chapter were carried out from COMSATS Institute of Information Technology.

4.4.1 The Van der Pauw Technique

Traditionally four point probe (4PP) is considered as standard measurements tool for resistivity characterization, however this technique provides no means of decoupling the effects of mobility enhancements and carrier density increases. Van der Pauw sheet resistance measurements were used as they avoid the penetration issues associated with the 4PP technique. In a 4PP measurement, the efficacy of the probe contacts is assured by weighting the probe arm. This results in penetration of the probe tips into the sample. As a result of the ultra-shallow nature of the implant profiles being investigated, this penetration can result in large errors in the measured sheet resistances. Van der Pauw measurements proceed through deposited ohmic contacts.

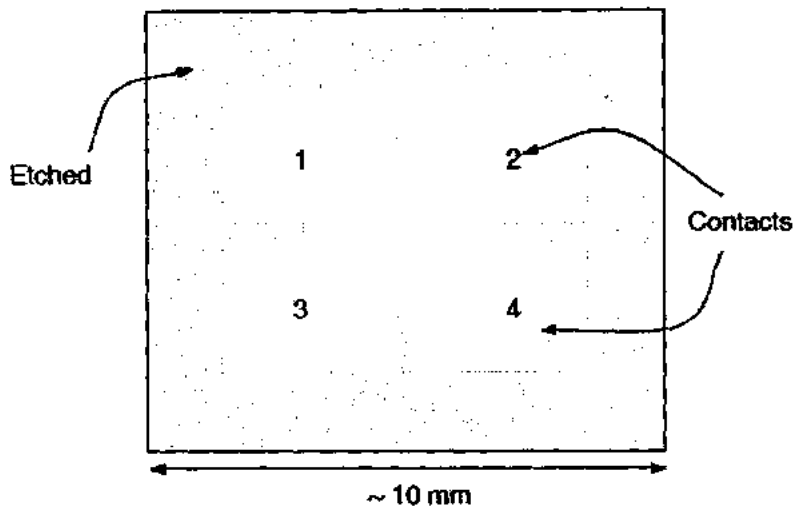


Figure 4.5: Cloverleaf pattern used to fulfill the criteria of Van der Pauw measurements.

The objective of the resistivity measurement is to determine the sheet resistance R_S. Van der Pauw demonstrated that there are actually two characteristic resistances when a current is applied between contacts 3 and 4 (I_{34}) and the associated voltage is measured across contacts 2 and 1 (V_{21}). The resulting resistance (RA) is then calculated $R_A = V_{21}/I_{34}$ and similarly when current is applied between contacts 4 and 2 (I_{24}) and the associated voltage is measured across contacts 1 and 3 (V_{13}). The resulting resistance (RB) is then calculated R_B-V_{13}/I_{24}, associated with the corresponding terminals shown in figure 4.5 R_A and R_B are related to the sheet resistance R_S through the van der Pauw equation [33]. The bulk electrical resistivity, ρ, can be calculated by using equation:-

$$\rho = R_S d \qquad (4.1)$$

If the sample geometry provides a line of symmetry between points 2 and 3 (as is the case in the cloverleaf structure), R_A and R_B will be equal and the sheet resistance becomes equal to:-

$$R_S = \pi R_A \times \frac{1}{\ln 2} \qquad (4.2)$$

The Hall measurements in the van der Pauw technique were carried out to determine the sheet carrier density, n_s by measuring the Hall voltage V_H. The Hall voltage is negative for n-type semiconductors and positive for p-type semiconductors. The Hall voltage measurement consists of a series of voltage measurements with changing current from 1 nA to 30 nA and a constant magnetic field 'B' of 0.37 Tesla is applied perpendicular to the plane of the sample. Once the Hall voltage V_H is acquired, the sheet carrier density n_s was calculated via $n_s=IB/q\,|V_H|$ from the known values of I, B, and q [33]. By using sheet carrier concentration and sheet resistance we determine the Hall mobility from the equation

$$\mu = \frac{V_H}{IBR_s} = \frac{1}{qn_s R_s} \tag{4.3}$$

$$\mu = \frac{R_H}{R_s} \tag{4.4}$$

The conducting layer thickness d is known, so we determine the bulk resistivity ($\rho=R_S d$) and the bulk density ($n = n_S/d$) [32]. The data obtaining from Hall measurement System HMS3000 is shown in figure 4.6.

4.4.2 Semiconductor Characterization System Keithley Model 4200

The results for electrical characterizations were also carried out by using Keithley Model 4200, because electrical characterization is important in determining how much the junction is efficient and behaves in different annealing regime. Keithley Model 4200-SCS Semiconductor Characterization System is able to simply test and analysis critical electrical measurements [35].

The Model 4200-SCS is well-suited for performing a wide range of measurements, including DC and pulsed current-voltage (I-V), capacitance-voltage (C -V), capacitance-frequency (C-f) because it is an integrated system that includes instruments for making DC and ultra-fast I-V and C-V measurements, as well as control software, graphics, and mathematical analysis capability. Keithley's Model

4200-CVU instrument comes as a module that plugs into any available instrument slot of the Model 4200-SCS Semiconductor Characterization System, allowing fast and easy current and capacitance measurements from femto-Farads to nano-Farads, at frequencies from 10 kHz to 10 MHz. Developed with the most modern and high performance circuitry available, the Model 4200-CVU design provides intuitive point-and-click setup, simple cabling, and built-in element models that eliminate the guesswork in obtaining valid C-V measurements. Good for advanced CMOS pulse I-V testing and high speed single pulse charge trapping [36]. Sheet resistance was measured for as implanted and annealed In+C co-implanted silicon and boron implanted silicon.

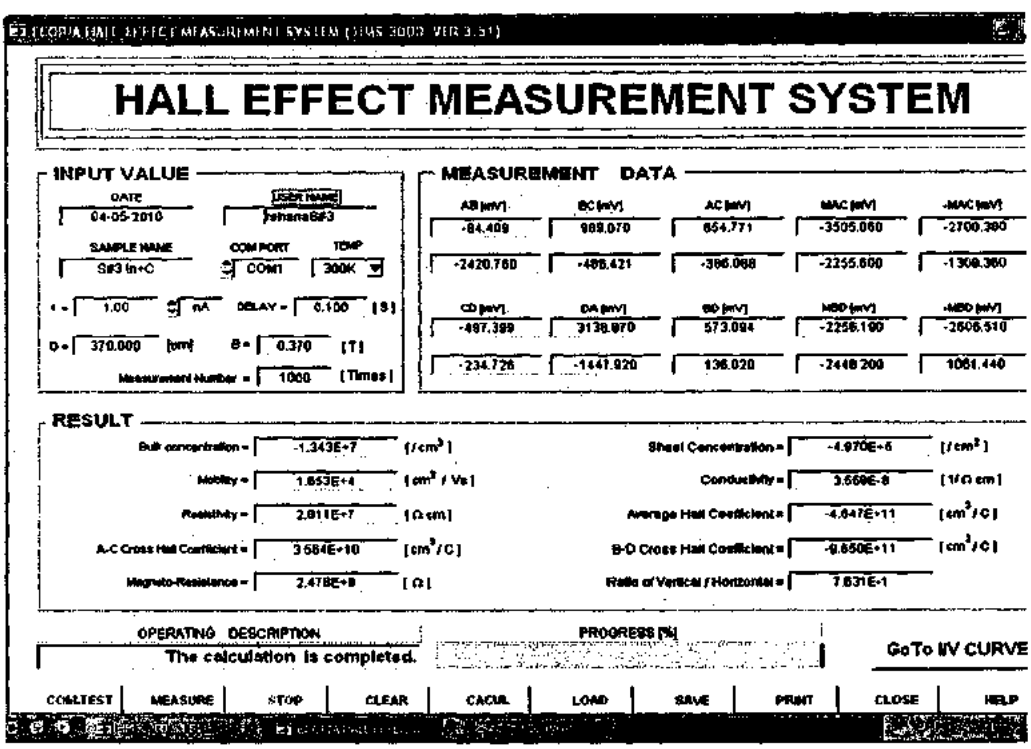


Figure 4.6: Data sheet obtained from Hall Measurement System HMS3000 for as-implanted In+C co-implanted Si substrate.

4.4.3 CV Measurement Technique

Electrical measurements have also been performed on a Material Development Corporation (MDC) Probe Station equipped with a Keithley 237 voltage

source/picoammeter and an Agilent 4980A precision LCR meter. This set-up is computer controlled by the MDC software package CSM/Win Quiet CHUCK. The CV plotting system is customized with the above mentioned MDC mercury probe, hot-chuck and with a capacitance–voltage meter that performs measurements using a low frequency measurement method as shown in figure 4.7. The CV-plotting system includes components such as an output device, memory (random access memory, read only memory, a hard disk drive), and a processor or CPU. The processor is in communication with the memory, capacitance–voltage meter and with the output device.

The desired output devices can be employed in the CV plotting system (printer, plotters and network devices) to report, store, graph or transfer the measurement data. The capacitance voltage meter has two electrodes or terminals for connection to a probe, a force electrode or terminal and a sense electrode or terminal. These electrodes are connected to a probe station which acts on a semiconductor wafer to obtain electrical measurements. One of the electrodes is connected to an area that is much larger than the area of the mercury tip and faces semiconductor wafer [38].

Then capacitance voltage measurement is taken by using low frequency measurement method and quasi static measurement method. In this work MDC /CSM is chosen because we can get high resolution at the probe tip (DC biasing down to milli-volts and capacitance measurement down to femto-farads) and can measure Low capacitance (pico-farad and smaller values) [37,38]. By using this system Sheet resistance, doping concentration and junction depths were measured for as-implanted and annealed In+C co-implanted and boron implanted n-type silicon.

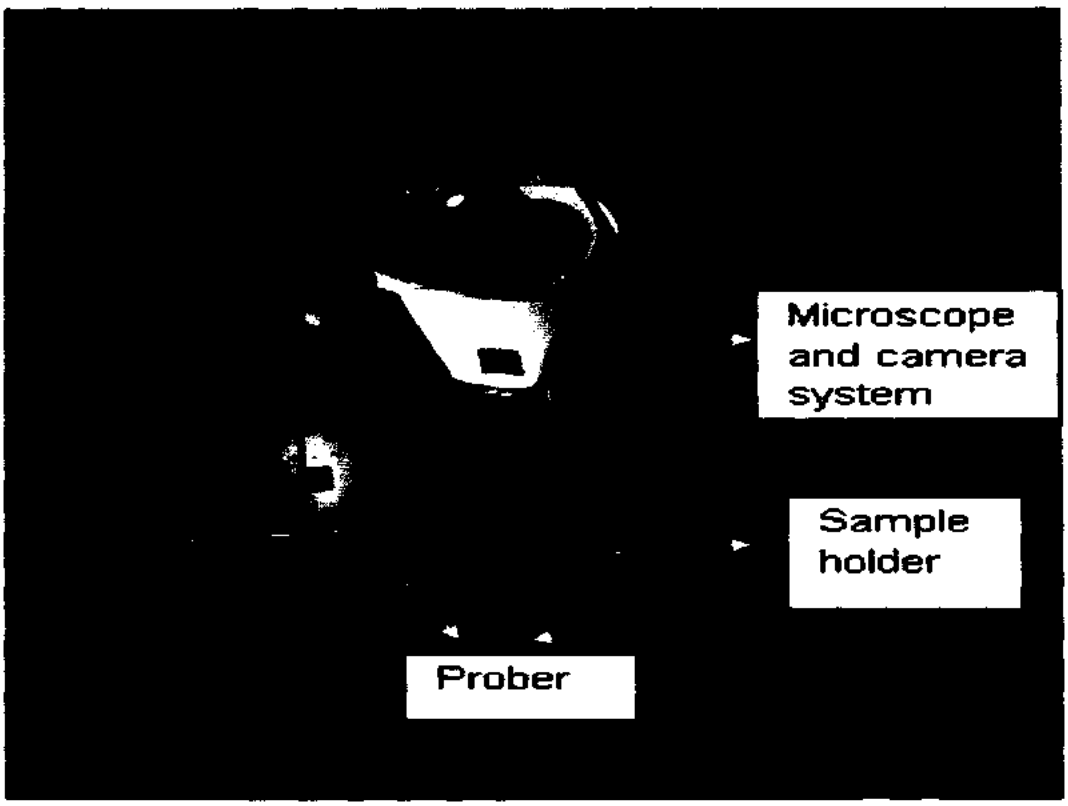


Figure 4.7: Probe station used for I-V & C-V measurements [38].

4.5 Setup and Measurements of Ellipsometry

Within this research work, greater emphasis is placed on the formation of junction and effect of annealing temperature on behavior of junction. For this purpose Ellipsometry is used as a characterization tool to measure junction depth and optical parameters (refractive index, extinction coefficient, dielectric function and absorption coefficient) of established abrupt ultra shallow junction, because spectroscopic Ellipsometry is one of the best non-contact, non-destructive tool to study the optical properties of such junctions. We use a compensator to optimize the measurements data especially for the USJ on bulk where we require the maximum sensitivity. The optical data pertaining to this work has already been published [39]. In this work, the optical characterizations were carried out using a rotating compensator Ellipsometer, which was proposed by J.A. Woollam (commercial J. A. Woollam Co., Inc. M-2000VI multichannel Ellipsometer covering the visible to near infrared spectral region). The

measurements reported in this chapter were carried out from COMSATS Institute of Information Technology and NILOPE, Islamabad

The electro-optical measurements were performed at room temperature with a rotating compensator Ellipsometer, the M-2000VI spectroscopic Ellipsometer, which is the first Ellipsometer to truly excel at everything from in-situ monitoring and process control to large-area uniformity mapping and general purpose thin film characterization [40].

It is based on advanced Diode Array Rotating Compensator Ellipsometer (DARCE), which provides consistently accurate Ellipsometric data. It delivers both speed and accuracy and can collect the entire spectrum (hundreds of wavelengths) in a fraction of a second with a wide array of configurations. This M-2000 Vlr multichannel Ellipsometer, which is mounted on an automated stage as shown in figure 4.8 consists of a polarizer, rotating compensator and a 50 W halogen lamp. Standard measurement parameters of rotating compensator Ellipsometer are used and the angle of incidence is set at 70°. When light passes through a rotating compensator after reflection from the sample (In+C co-implanted Si) surface, is spectrally separated by a prism and directed towards the CCD arrays. CCD camera fed these images to the computer, which perform pixel by pixel intensity analysis and generates Ellipsometric data for each point, so in this way we collect two dimensional mapping of a junction as shown in figure 4.9. It consists of two CCD arrays, one CCD array can collect 200 wavelengths between 1000 to 1690 nm and other CCD array can detects a total of 390 wavelengths within spectral range of 371 to 1000 nm. It also consist controlled z-alignment, which is used for sample height adjustment. The motorized goniometer is also mounted with horizontal sample stage enables angle resolved measurements (ψ=0-90°, Δ=0-360°). As shown in figure 4.8. WVASE32 software is used for the analysis of data.

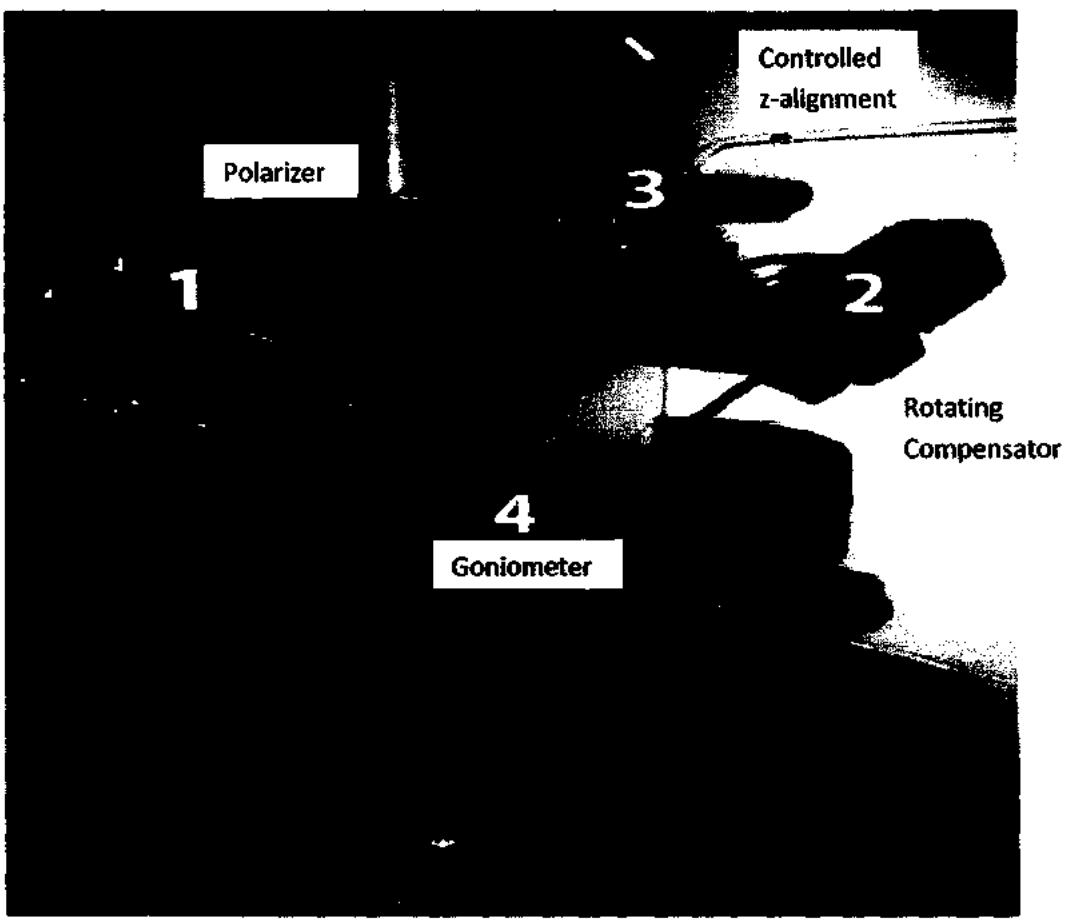


Figure 4.8: M-2000VIr multichannel Ellipsometer mounted on an automated stage [40].

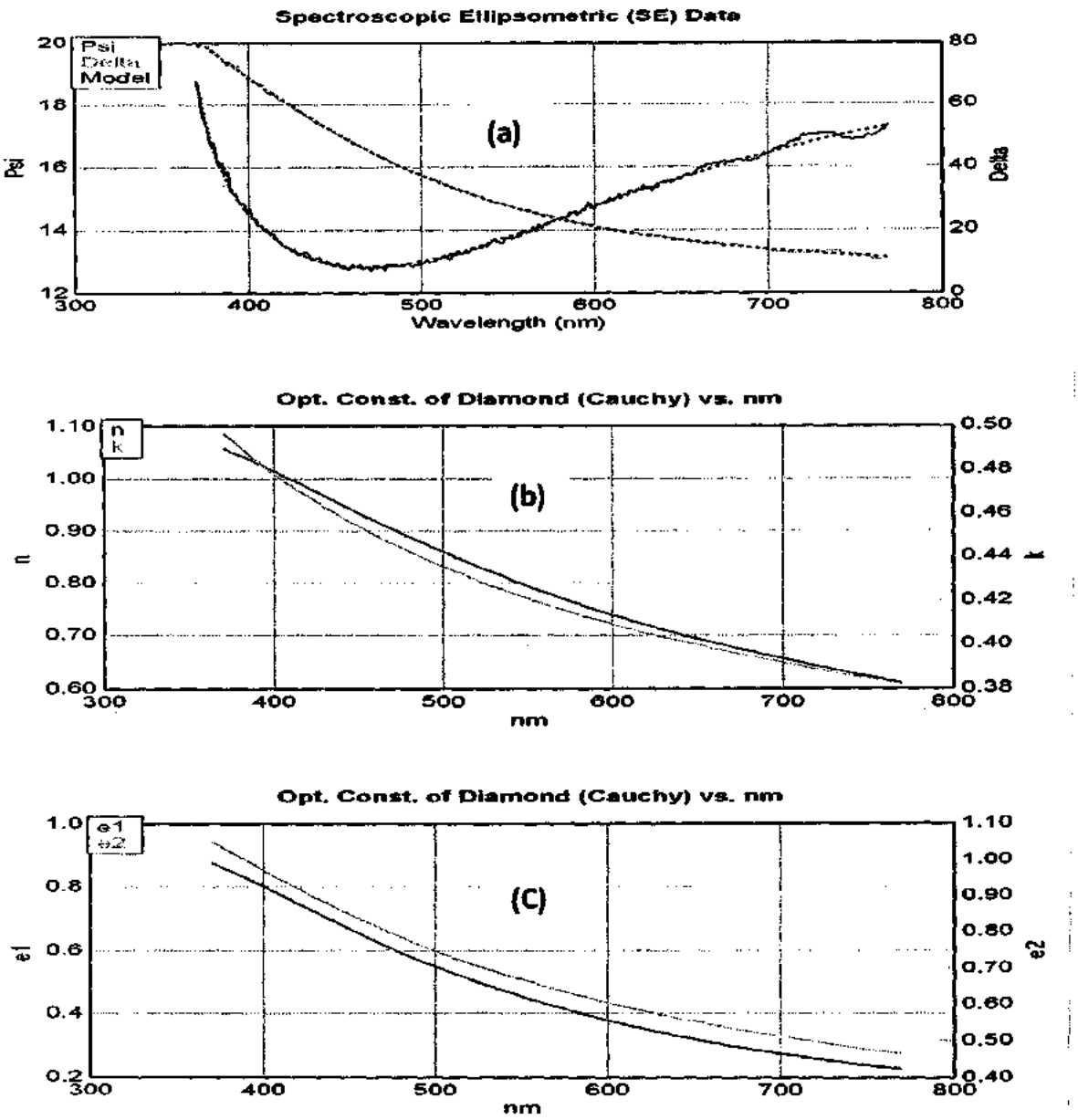


Figure 4.9: Ellipsometric results showing (a) Psi and delta versus wavelength (b). Real and imaginary parts of refractive index versus wavelength (c) Real and imaginary part of Dielectric function for as implanted In+C co-implanted Si substrate.

4.6 X-Ray Diffraction Measurements

In order to fully optimize the test process and fabrication strategy, a controlled behavior of tailored films and surfaces on atomistic level is required to ascertain process yield and manufacturing cost. X-rays (in various forms such as XRD, XRF, X-rays scattering measurements etc.) are widely used in semiconductor manufacturing industry to examine, evaluate, and analyze the surfaces, interfaces, thin films and device regions. XRD, in particular, has emerged as standard diagnostic technique for structural investigation in ion implantation technology particularly to study the stress, strain and distortion created in the ion implanted layers due to the creation of point defects and/or extended defects in the crystal. Some End-of-Range (EOR) defects may reportedly be responsible for the clustering of silicon interstitials in this region where indium dopant profile dominates in the Si matrix [52, 53, 54].

Within this research work, little emphasis is placed on the strain levels within the active "-Si layer and their response to surface modification through ion-implantation and annealing processes. In order to monitor these strain levels x-ray diffraction (XRD) is used because X-ray diffraction (XRD) is a versatile technique primarily used for phase identification of a crystalline materials and can provide information on chemical composition and unit cell dimensions of manufactured and natural materials. XRD facilities in CIIT, Islamabad has been used to measure the extent of structural morphology caused due to ion irradiation of the samples particularly with reference to the USJ formation in the area/depth of our interest of these samples. The data pertaining to this technique has been published [85].

In our case X-ray measurements were done with the help of a Siemens D-500 X-ray Diffractometer and a Philips X, Pert machine. From the X-Ray data the strain is calculated. X-ray diffraction is based on constructive interference (when conditions satisfy Bragg's Law ($n\lambda=2d \sin\theta$) of monochromatic X-rays and a crystalline sample.

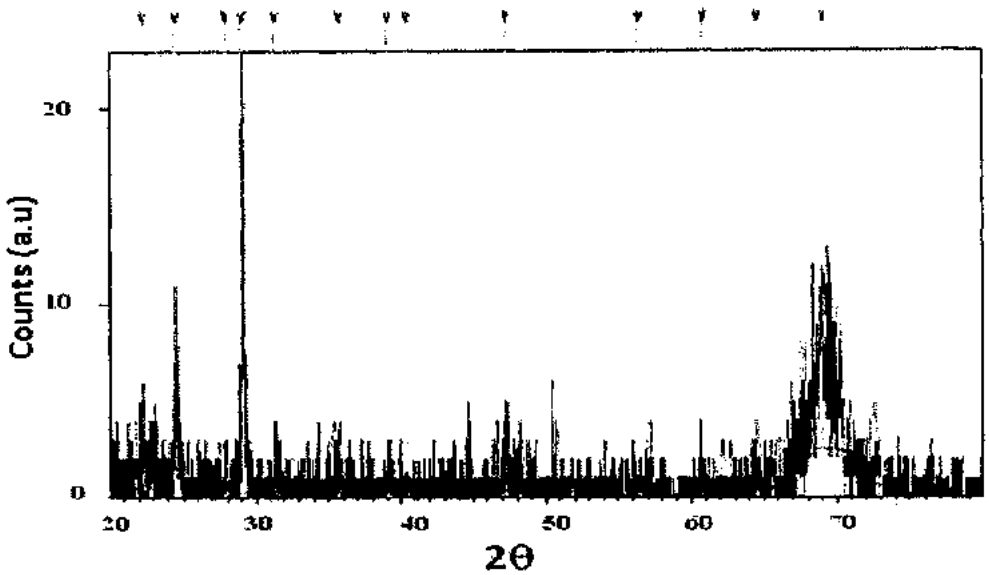


Figure 4.10: XRD spectrum obtained for In+C co-implanted n-type Si substrate

Table 4.3: Shows d-spacing, FWHM and relative intensities of figure 4.10 at 2θ positions. (Peak List)

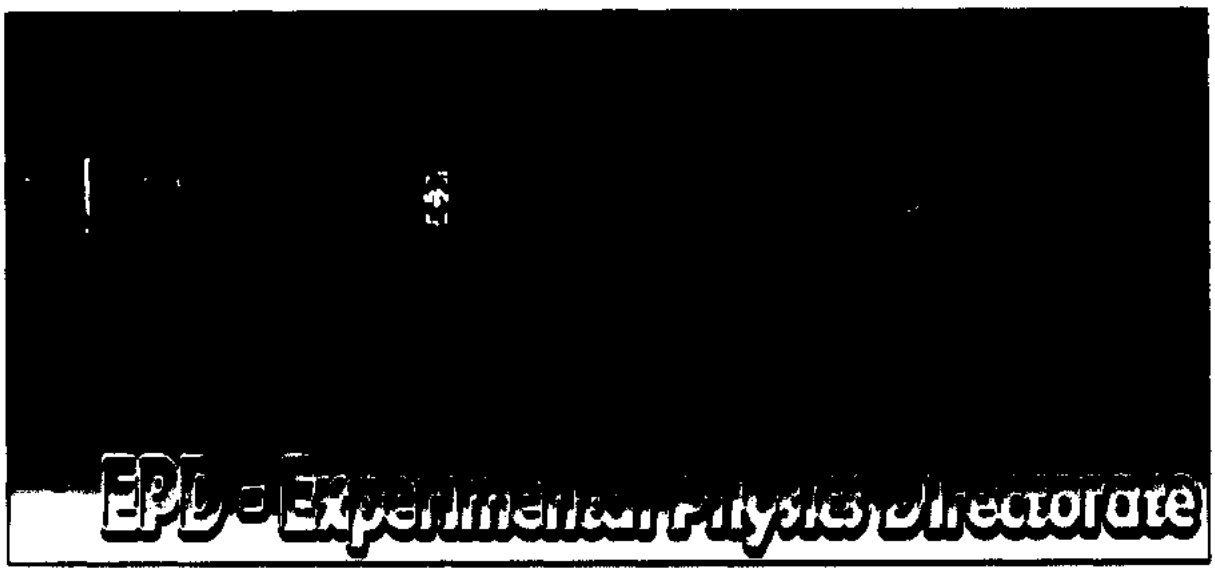
Pos.[°2Th.]	Height[cts]	FWHM[°2Th.]	d-spacing[Å]	Rel.Int.[%]
22.2383	1.12	0.9446	3.99760	6.87
24.5168	5.98	0.2362	3.63100	36.62
27.8846	0.84	0.1968	3.19965	5.15
29.0660	16.32	0.1574	3.07222	100.00
31.3174	0.90	0.4723	2.85632	5.52
35.7016	2.59	0.1181	2.51497	15.90
39.0541	1.50	0.2362	2.30645	9.19
40.3667	3.11	0.0590	2.23443	19.07
47.2645	1.80	0.3936	1.92319	11.05
56.4010	0.48	0.6298	1.63141	2.91
60.7914	0.73	0.3936	1.52369	4.49
64.4952	1.07	0.3149	1.44484	6.55
69.0171	5.76	0.7680	1.35968	35.27

X-rays are generated in a cathode ray tube by heating a filament to produce electrons these are filtered to produce monochromatic radiation. By applying voltage electrons are accelerated towards the target. X-ray spectrum was produced when electrons have sufficient energy to dislodge inner shell electrons of the target material. The spectra were recorded and intensities were measured for further analysis.

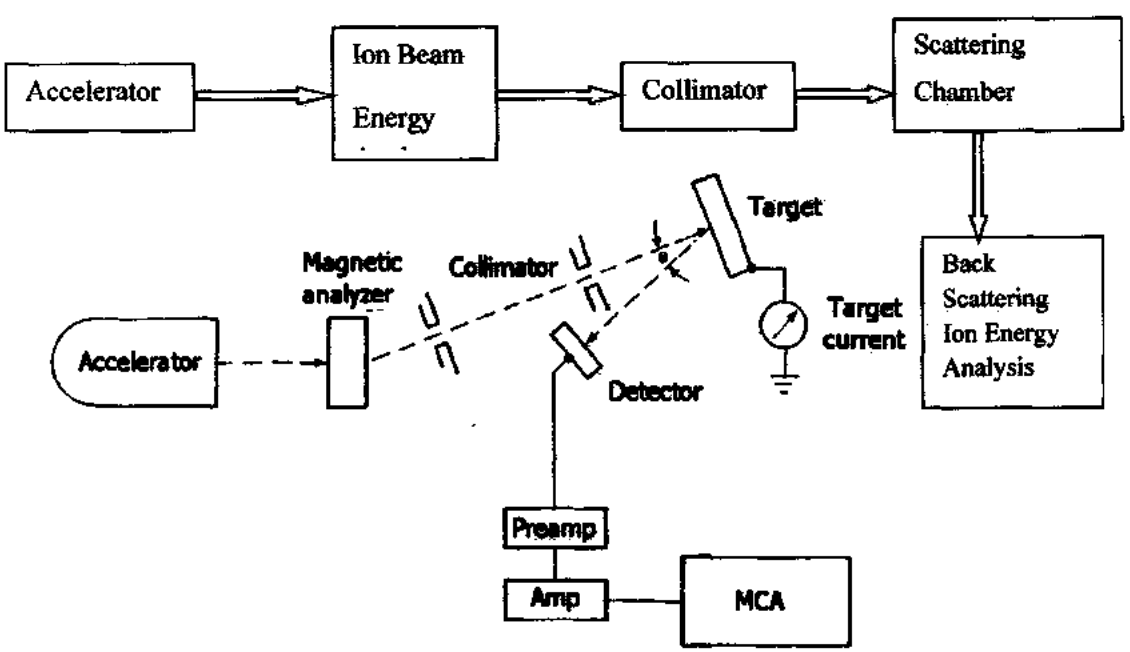
4.7 Rutherford Back Scattering Spectroscopic Setup and Measurements

Rutherford Backscattering Spectroscopy (RBS) is a powerful technique for the qualification of USJ samples. RBS has become a regular testing technique in the running fabrication plants for indirect investigation of thickness and atomic distribution (FABs) where CMOS transistors with decreasing scaling of junction depth are manufactured. Keeping this very fact in mind, we have tested our samples against RBS protocols. The light dopant composition and depth profiles obtained by RBS technique were studied together with the similar profiles obtained by Electrical measurements and ellipsometry. The first-ever 5 MeV accelerator of Pakistan commissioned in National Centre for Physics (NCP) has also been rigorously used to develop special protocols for our characterization experiments. The data pertaining to this measurement is published [39].

In this experiment 5 MeV Tandom accelerator is used, where He charged particles are generated in an ion source. Their energy is then raised to several mega electron volts by an accelerator. This high energy beam then passes through a series of devices which collimate and focus and then filter it for a selected type of particles and energy like a magnetic field separates any He^-, He, or He^+ from the He^{++} beam. A quadrupole lens shapes the beam and focuses it into the sample chamber. The beam then enters the scattering chamber and impinges on the sample to be analyzed.



(a)



(b)

Figure 4.11: (a) Illustration of accelerator in NCP. (b) Schematic of accelerator used for Rutherford Back Scattering Spectrometry [110].

The energy of these backscattered particles (governed by the kinematic factor) provides information regarding the mass of the host atom from which the scattering event has occurred, which then provides a mass scale. At the same time the rate of energy loss of the ions, combined with knowledge of the stopping power cross- sections of He in the matrix, provides a depth scale. We can then derive concentration vs. depth from the resulting spectra. In all cases the beam was normal to the sample. The scattered particles were analyzed with a solid state detector located about 10 cm from the target with a solid angle 2.74 msr. The detector resolution is between 15 and 20 keV.

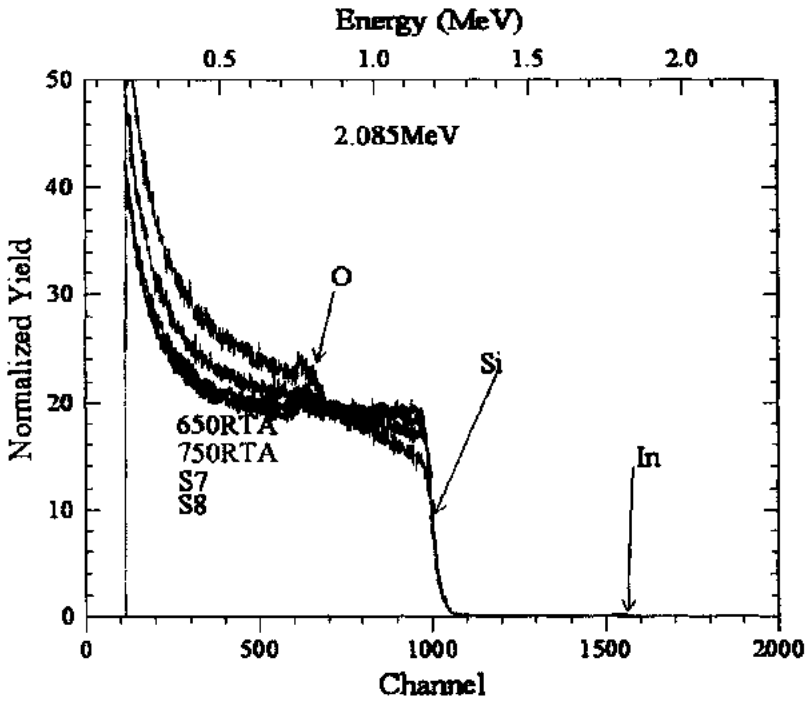


Figure 4.12: RBS spectrum recorded for He^{++} ions incident on the In+C co-implanted n-type Si substrate showing a comparison of as implanted and annealed results of RBS yield. The Si, C and In peaks are identified.

For the analysis of In+C co-implanted silicon substrate and n-type boron implanted silicon substrate 2-4 MeV He^{++} ion beam has been used with scattered angle ϕ=170°.

Some of the backscattered particles impinge on the detector, where they generate an electrical signal the energy spectrum of these backscattered He^{++} ions is recorded as shown in figure 4.12. The energy loss of the He ions is predominantly inelastic but there are occasional elastic collisions (~ ne in 4000) resulting in a backscattering event. All the spectra were recorded under routine experimental conditions on Tandom Accelerator facility in National Center for Physics, Islamabad. Illustration of the NCP RBS facility is shown in figure 4.11(a) and schematic of its experimental setup is shown in figure 4.11(b).

4.8 Grazing Incidence X-Ray fluorescence Setup and Measurements

In the present work, an approach for the characterization of USJ by using synchrotron radiation-induced GIXRF analysis is used as a cross- check method for the junction depth measured by CV System, Ellipsometry, and RBS characterization techniques. The data pertaining to this work has been submitted [112]. The measurements reported in this chapter were carried out from Lawrence Berkeley National Laboratory, California, USA. Although SIMS (secondary ion mass spectrometry) is the most common method used in the semiconductor industry for deph profiling because even traces of elements and micro-regions can be investigated but troublesome matrix effects can occur which require sophisticated quantification procedures.

Another well known technique for depth profiling, Rutherford backscattering spectrometry (RBS) is non-destructive but has a poorer depth resolution and is not very sensitive [63]. Then there is a need for analysis techniques, complementary to secondary ion mass spectrometry (SIMS), for depth profiling of dopants in silicon for ultra-shallow junction (USJ) applications in CMOS technologies. A recently emerging technique Grazing Incidence X-Ray Fluorescence (GIXRF) in the soft X-Ray range is an alternative to SIMS is a high potential tool for this purpose that is non-destructive and only suitable for thin layers up to some 30 nm. In this case, the dopant concentrations are sufficiently high and close enough to the surface so GIXRF analysis is completely feasible [64].

The GIXRF measurements were carried out at the XRF Fluorescence beamline 11.0.1 of the Advanced Light Source (Lawrence, Berkeley) by using a monochromatic X-Ray beam of 180, 188 and 195 eV and endstation 11.0.1.2.as shown in Table 4.4. The setup includes micro meters and 4 mm slits limiting the beam size on the sample mounted on a high precision goniometer. Angular scans are performed in around the critical angle of θ-2θ at beam energies 280 and 290 eV. This beamline provides monochromatized 5cm elliptical polarization undulator radiation in the photon energy range from 150 to 2000 eV. After the angular scan fluorescence emissions were collected at different grazing angles by using Si(111) channel-cut monochromator. After this the incident beam intensity and the energy calibration were monitored using an ion chamber and an indium (In), or carbon (C) metal standard, then X-Ray penetration depth for each incident angle was estimated by using X-Ray database of Lawrence Berkeley National Laboratory. The data obtained is shown in figure 4.13.

Table 4.4: Parameters set for GIXRF measurements

Beam Line	11.0.1
Source Characteristics	5.0 cm-period elliptical polarization undulator
Energy Range	150-2000 eV
Monochromator	VLS-PGM
Energy Resolution	4000 at 800 eV
Endstation	Soft X-Ray Scattering 11.0.1.2
Detectors	In-vacuum CCD, Photodiode
Spatial Resolution	>2nm
Calculated flux	$10e^{13}$ photons per second

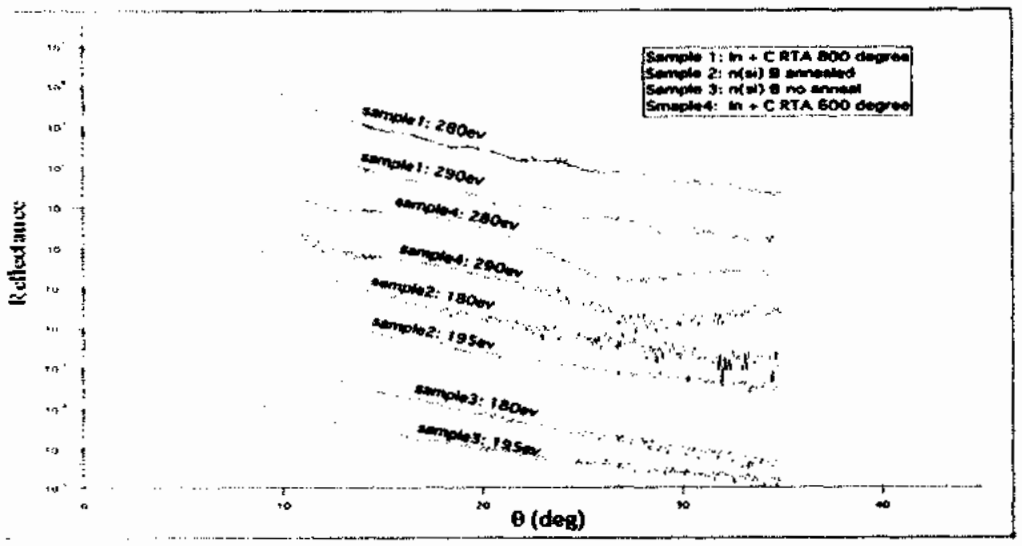


Figure 4.13: GIXRF spectrum recorded for In+C co-implanted n-type Silicon substrate and B implanted n-type Si substrate.

Grazing incidence XRF, which is used here as the analytical method, was first used to significantly reduce scattering background contributions when analyzing small amounts of material on top of a flat support [116]. This corresponds with total reflection XRF, where the incident angle is well below the critical angle for total external reflection. Since then, GIXRF has been widely used for the analysis of periodic multilayers [117], adsorbed molecules [118] as well as thin layers [119] on substrates. Dopant profiles have also been the subject of nondestructive analysis with GIXRF [120] in the hard X-ray range.

An alternative approach towards dopant depth profiling using GIXRF has recently been developed by Steen et al. [121, 122]. TXRF, total reflection of the exciting radiation is realized by a shallow angle of incidence between X-ray beam and sample surface. This angle should be well below the critical angle θ_{crit} for total external reflection, which is a photon energy- and material-dependent parameter [123]. In this process, when X-rays are absorbed by matter, electrons are excited from core levels into unoccupied states, leaving empty core states. Secondary electrons are generated by the decay of the core hole.

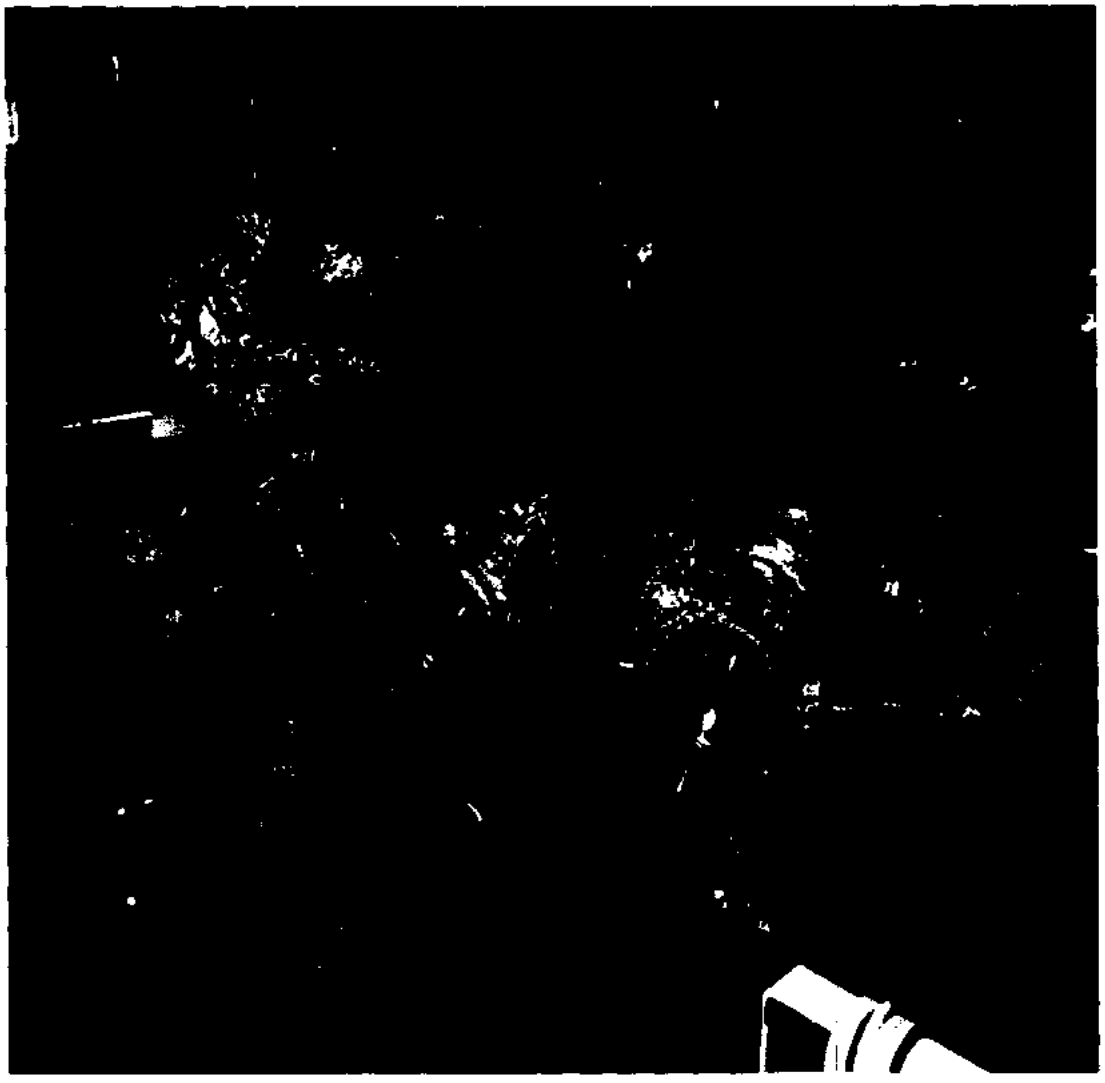


Figure 4.14: End Station GIXRF [111].

So Auger processes and inelastic electron scattering create a cascade of low-energy electrons of which some penetrate the sample surface, escape into vacuum and are collected. Electrons emitted from sample in response to the absorption of ionizing radiation. These electrons are accelerated by a strong electric field. This wide electron distribution is the principal source of image. Electrostatic and magnetic deflectors are used for beam-steering and shaping and dipole separator magnet directs the electron beam into the projector optics as shown in figure 4.14.

By applying such a setup, penetration of only the first few nanometers of the sample can be achieved, resulting in a low scattering background in the spectra detected. In GIXRF, the angle of incidence is varied around the critical angle for total external reflection θ_{crit}. In this work, values between 0 and 35° were used to modify the characteristics of the X-Ray Standing Wave field (XSW) field, leading to a deeper penetration into the sample as the angle of incidence θ increases. In GIXRF, the penetration depth as well as the intensity distribution of the incident radiation inside the sample is strongly dependent on the angle of incidence and the photon energy. Thus, the measured fluorescence radiation of the elements of interest is also an angle dependent quantity. This enables us to measure the depth-dependent quantification of layers or elements.

4.9 Atomic Force Microscopy (AFM)

The aim of using this technique is the measurement of behavior of roughness after implantation and thermal annealing, because The AFM is one of the foremost tools for imaging, measuring, and manipulating matter at the nano-scale. Atomic Force Microscopy facility present in CIIT, Islamabad (AFM Agilent system 2500 picoscan) has been used to image the extent of surface roughness caused due to ion irradiation of the samples particularly with reference to the USJ formation in the area/depth of our interest.

The surface morphology of implanted annealed samples was carried out using Atomic Force Microscopy. The AFM probes the surface of a sample with a sharp tip, a couple of microns long and often less than 100 Å in diameter. The tip is located at the

free end of a cantilever that is 100 to 200 μm long. Forces between the tip and the sample surface cause the cantilever to bend, or deflect. A detector measures the cantilever deflection as the tip is scanned over the sample, or the sample is scanned under the tip. The measured cantilever deflections allow a computer to generate a map of surface topography. Several forces typically contribute to the deflection of an AFM cantilever.

The force associated with atomic force microscopy is an inter-atomic force called the van der waals force. The dependence of the van der Waals force upon the distance between the tip and the sample is in the contact regime, in this regime the cantilever is held less than a few angstroms from the sample surface, and the inter-atomic force between the cantilever and the sample is repulsive. In the non-contact regime, the cantilever is held on the order of tens to hundreds of angstroms from the sample surface, and the inter-atomic force between the cantilever and sample is attractive (largely a result of the long-range van der Waals interactions) [125].

The informations were gathered by "feeling" the surface with a mechanical probe. Piezoelectric elements that facilitate tiny but accurate and precise movements on (electronic) command enable the very precise scanning. In some variations, electric potentials can also be scanned using conducting cantilevers. In newer more advanced versions, currents can even be passed through the tip to probe the electrical conductivity or transport of the underlying surface. These informations were transferred to the computer and will be converted to three dimensional images of surface roughness [69]. The representative results are shown in figure 4.15.

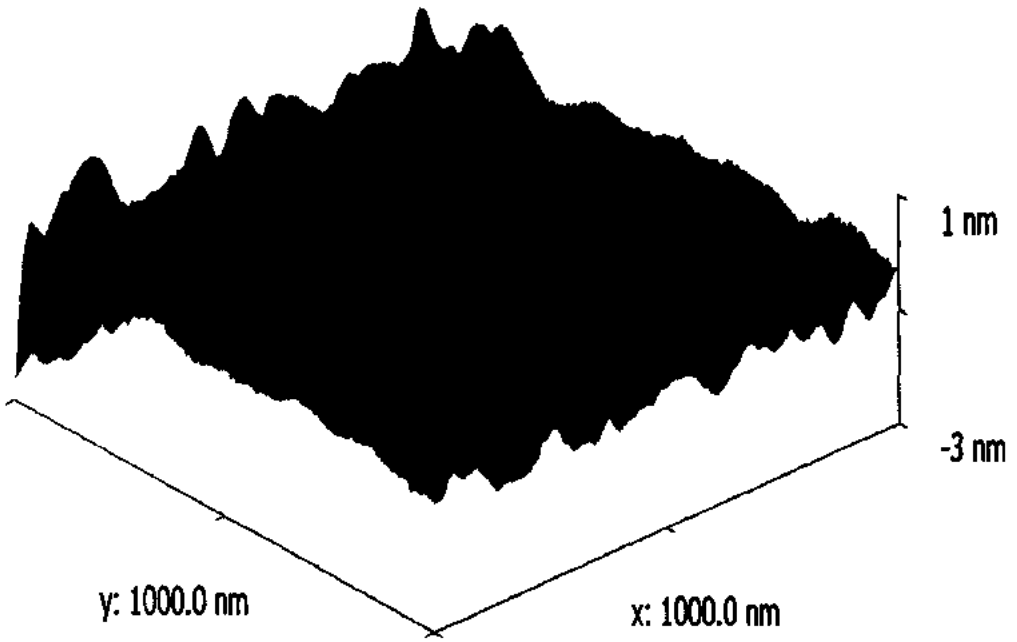


Figure 4.15: Atomic Force Microscopic topographical view of the In+C co-implanted Si Substrate before annealing showing extent of roughness and uniformity of the deposited indium and carbon co-implants. The presence of impurity concentration of boron and phosphorous at different depths is also visible as background structural information. This three dimensional view shows negligible degradation of the morphology of the surface after the devised and processed implant strategy.

Chapter No. 5

This chapter comprises two parts. First part describes the characterization results of In+C co-implanted Silicon substrates obtained from different characterization techniques. The second part describes the characterization results of boron implanted n-type silicon substrate obtained from different characterization techniques.

5.1 Analysis of Simulated Results

In order to find out the resultant range and damage profile in the Si substrate due to indium and carbon ions, rigorous simulations were performed with various ion energies at different incident angles' a computer code Stopping and Range of Ions in Matter was used for the present work. Further, Silvaco TCAD code was used to predict the distribution of defects in the Si substrate due to the carefully chosen ion implant schedules. These simulations constitute the central part of the work, because very careful parameter optimization is required to study the process sequence to fabricate ultra-shallow junctions. These simulations are also very important to compare the characterization data with the simulated ones in order to generate a workable model for actual devices.

The results of the Stopping and Range of Ions in Matter (SRIM) simulations selected for the fabrication of the device are shown in figure 5.1. Figure 5.1 exhibits carefully simulated positions of the combined indium plus carbon ion implantation in n-type Si. The peak concentration of 9.8×10^{20} atoms/cm^3 appears at the depth of 34 nm in silicon with a straggle of ± 4.86 nm as tolerance. Our experimental results show that junction formation occurs near about simulated junction depth (shown by a vertical line) in figure 5.1. The position of the junction, for the as implanted is 40 nm and vary from 10 nm to 60 nm due to the variation in annealing temperature. In the area of ion implantation, predictive TCAD modeling is needed to get accurate physical modeling of the implant processes. TCAD is excellent for ultra-low energy implants. The result of SILVACO TCAD simulations for the response of the defects against annealing temperature are plotted in figure 5.2.

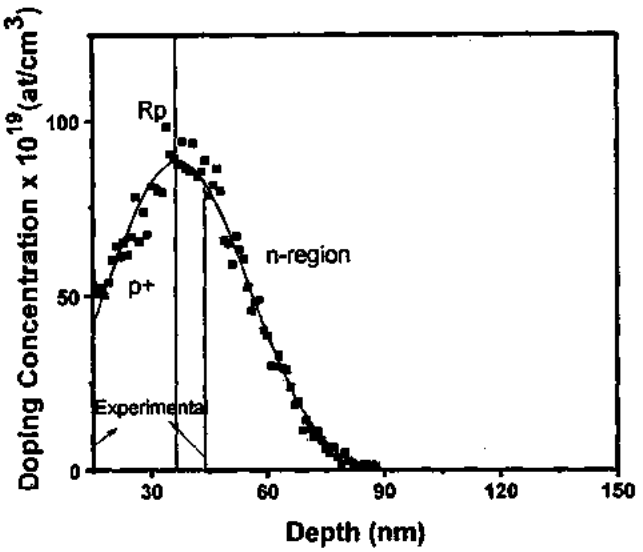


Figure 5.1: Simulated positions of the combined implanted indium and carbon atoms showing atomic concentration profile at different depths in silicon substrate. The n-type Si substrate is implanted with indium and carbon ions at 70 keV and 10 keV, respectively with respective doses of 5.7×10^{14} ions cm^{-2} and 3.4×10^{15} ions cm^{-2}. The simulations were carried out by SRIM-2011 code. The vertical line shows the projected range. The experimental results show that the position of the junction moves from 17 to 43 nm due to variation in annealing temperature.

The result of SILVACO TCAD simulations for the response of the interstitial atoms against annealing temperature is shown in figure 5.2. Window of this graph is intentionally chosen up to 400 nm to explicitly study the behavior of active atoms and defects (generated due to co-implantation in the n-type silicon with carefully selected energies, doses and angles) in and around the vicinity of the activated junction areas. The representative curves shown in figure 5.2 is one of the sample undergone rapid thermal annealing cycle at 600°C. It is interesting to note that the net vacancy profile remains constant throughout the active device region, whereas an appreciable amount of net interstitials is present in and around the junction depth. The decrease in the interstitials (beyond the junction depth) in the bulk of the material is found with the increasing depth into the material, which suggests a very crucial role of these interstitials in forming a stable ultra shallow junction near the regions where impact of

peak concentration of indium and carbon atoms is visible and predominant. Keeping in view the provision of natural migration of active atoms and defect sites from surface to bulk, during the annealing processes an estimated 42 nm of the junction depth with reasonable number of active dopants at relatively low thermal budget provides a promising implant-annealing protocols to obtain a much controllable process window for variety of junction related applications.

Figure 5.3 shows that maximum number of interstitials at temperatures (23, 600, 650, 700, 750, 800, 850, 900, 950, 1000, 1100°C) lies between window 10-80 nm above this thickness number of interstitials decreases. At about 735 nm 40% of the interstitials lost. By annealing at 1100°C number of interstitials remains constant after 735 nm, after this number of vacancies increases and in depth formation of interstitial–vacancy pair increases. This graph also shows that samples annealed at lower temperatures (600, 650, 700°C) have minimum number of interstitials at depth below 1500 nm, but by increasing temperature movement of number of interstitials towards depth increases. Interstitial rich region helps us to avoid In-V by annihilation of I-V recombination, which shows that conduction near the surface is due to interstitials.

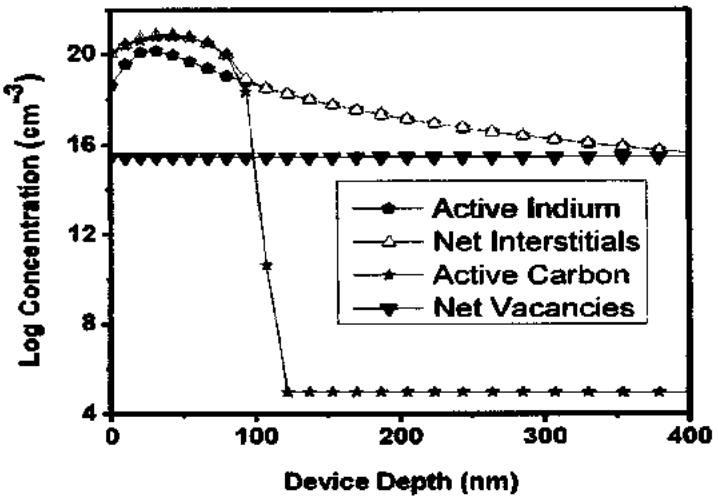


Figure 5.2: Graph showing number of interstitial atom, active indium, active carbon and net vacancies in silicon after post implant annealing at 600°C as representative temperature. These curves are simulated in device structure modeled by TCAD SILVACO.

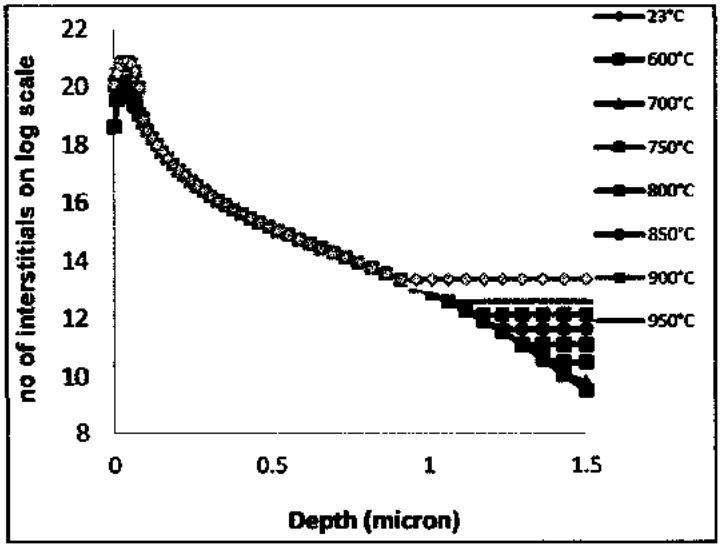


Figure 5.3: Behavior of interstitials of In and C in Si substrate at between annealing regime room temperature to 1100°C.

5.3 Description of Electrical Characterization

After the formation of the abrupt ultra shallow junction for In + C co-implanted silicon substrate of p-type and n-type conductivity annealed at different operational conditions, experiments were performed to carry out the electrical characterization of the above mentioned samples. Keithley 4200 I-V /CV System (especially tailored for reliable nano-regime measurements), MDC CSM CV system and Ecopia HMS 3000 Hall Measurement System were employed to determine the sheet resistance, sheet carrier concentration, mobility and resistivity of these devices to improve the tolerance and reliability of data (Van Der Pauw method was employed instead of the commercial four point probe, due to the shallowness of the junction and Au+Ge+Ag contacts were deposited on the surface through sintering process).

As we know that accurate sheet resistance measurements are important for the determination of the level of electrical activation, so sheet resistance of the samples was measured having junctions using three competitive techniques and the average values of repeated measurements range from~2.5×10^{2} to ~1.9×10^{4} Ω/square. The experimentally determined sheet resistance, sheet carrier concentration, mobility and depth of established junction of various implanted samples, both for as-implanted and annealed samples at different temperatures have been shown in figures 5.4 to 5.12. Figures 5.4, 5.6, and 5.12 show the sheet carrier concentration and mobility of the implanted samples as a function of annealing temperature again with the averaged values of repeated measurements in each case. In this experiment high annealing temperature is used instead of low temperature because at low temperature defects C_s-In_s responsible for the current conduction.

The presence of carbon in In+C co-implanted silicon substrate increases sheet resistance and decreases sheet carrier concentration than single indium implant. This is because in silicon carbon sits on substitutional sites by forming complexes with silicon interstitials, which shows that indium carbon co-implant exhibit reverse annealing behavior. So by using this recipe higher value of electrical activation can be achieved at lower thermal budget [127]. Sheet carrier concentration for the as-implanted In+C co-implanted silicon substrate is 4.97×10^{11} at/cm^2 and junction depth (Xj) 22 nm is

observed. When the samples were post annealed at different temperatures variations in junction depth, sheet resistance and sheet carrier concentration occurs. Due to indium intrinsic property indium atoms move upward causing decrease in junction depth. When the sample is annealed at 600°C, sheet carrier concentration increases and junction depth decreases, but a monotonic decrease of sheet resistance and drastic increase in junction depth is also observed from 600-650°C. Drastic decrease of sheet resistance is observed at 650-700°C. This suppression of sheet resistance is due to a reduction in the deactivation of the carrier concentration and improved mobility and increase in junction depth is due to the movement of indium atoms back to their original positions [128]. But a slightly different behavior is observed at an annealing temperature of 800°C. At 800°C, sheet resistance increases with parallel increase in sheet carrier concentration. This is because of the fact that at lower temperatures C-In defect formation occurs, which may be responsible for the current conduction. By increasing the annealing temperature, breaking of C-In complexes occurs owing the decrease of sheet carrier concentration and sheet resistance. With the further increasing temperature from 750-800°C as shown in figures 5.4 and 5.5, the complex of carbon with self-interstitial is stable and creates a region rich in defects, This results in deactivating the dopants by increasing the sheet carrier concentration and sheet resistance are according to the results as were experienced in earlier studies [129].

Figures 5.7 and 5.8 shows that by applying current of 5 nA we can get variable resistance between 10^2-10^3 ohm/sq and sheet carrier concentration between 10^{12}-10^{14} at/cm^3 at different annealing temperature ranging from 600-800°C. Figure 5.10 shows that by increasing the voltage current also increase. But by annealing In+C co-implanted Si substrate at 600°C current increases 10 times, which is due to the reduction in junction depth and sheet resistance. As activation of dopant atoms is critical for ultra shallow junctions, we also determined the activation energy for dopant atoms using Arrhenius plot of activation energies for In+C co-implanted Si substrate at different annealing temperatures. It has been found that for this implant recipe, almost 172 meV energy is needed to activate the dopant atoms after co- implantation in n-type Si substrate to form an effective and reliable ultra shallow junction.

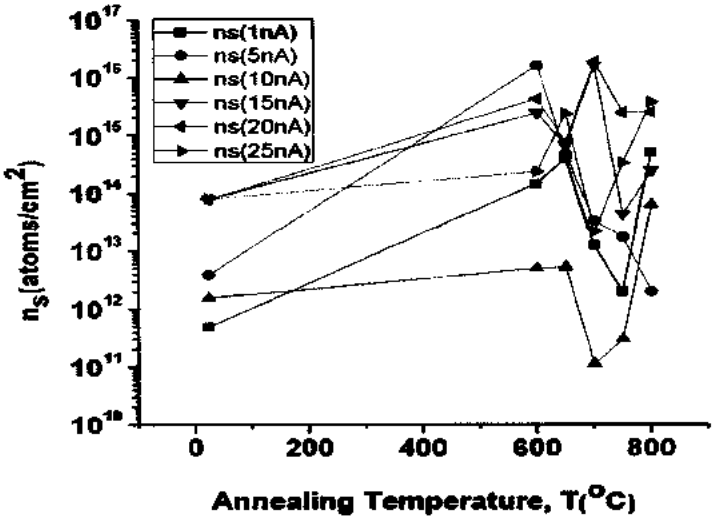


Figure 5.4: Plots showing variation of retained sheet carrier concentration with respect to annealing temperatures at different current ranges for In+C co-implanted n-type silicon substrate, again the data plotted here is obtained from Hall Measurement System HMS 3000.

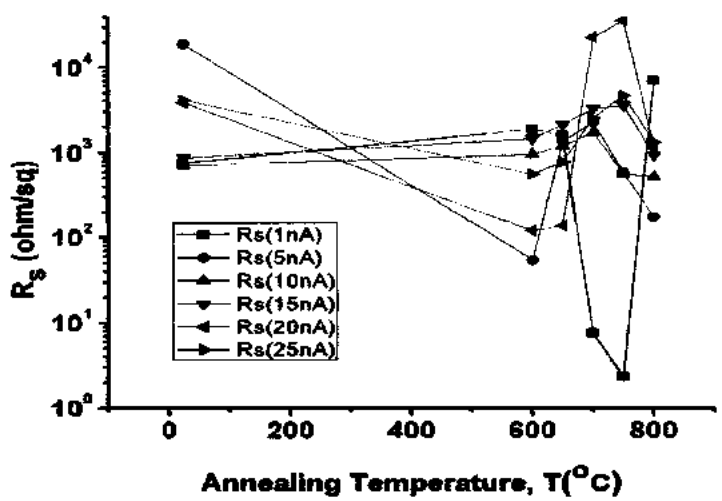


Figure 5.5: Variation of sheet resistance obtained from Hall Measurement System, for In+C co-implanted n-type silicon substrate against annealing temperatures from 600°C-800°C. The values plotted here are averaged against the data obtained after repeated measurements for each sample to assure the reliability and tolerance.

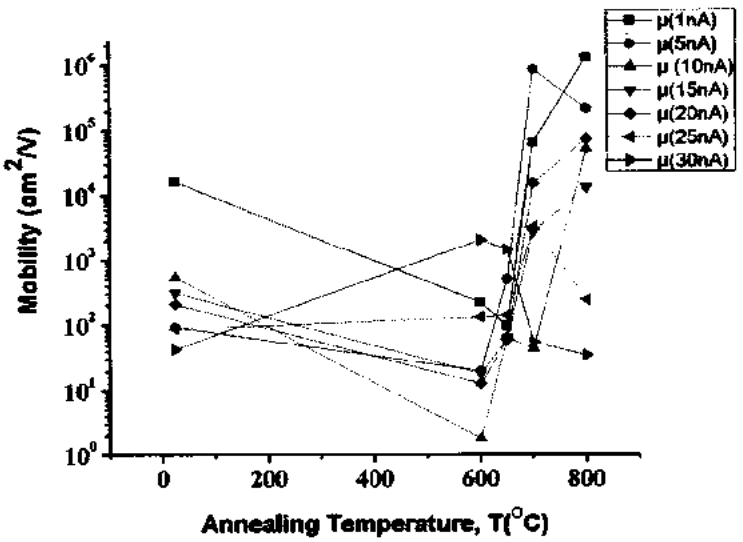


Figure 5.6: Plots showing variation of carrier mobility with respect to different annealing temperatures at current range from 1 nA-30 nA for In+C co-implanted n-type silicon substrate. Again, the data plotted here is obtained from Hall Measurement System HMS 3000.

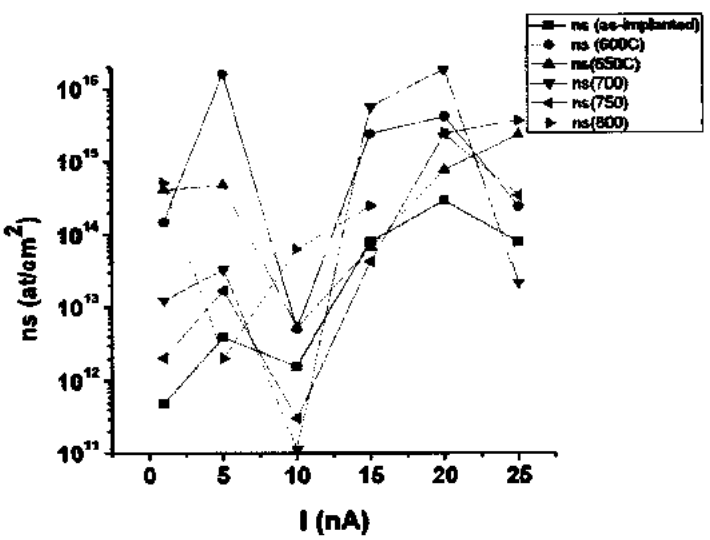


Figure 5.7: Plots showing variation of retained sheet carrier concentration with respect to current ranges from 1 nA-25 nA for In+C co-implanted n-type silicon substrate at different annealing temperatures. Again, the data plotted here is obtained from Hall Measurement System HMS 3000.

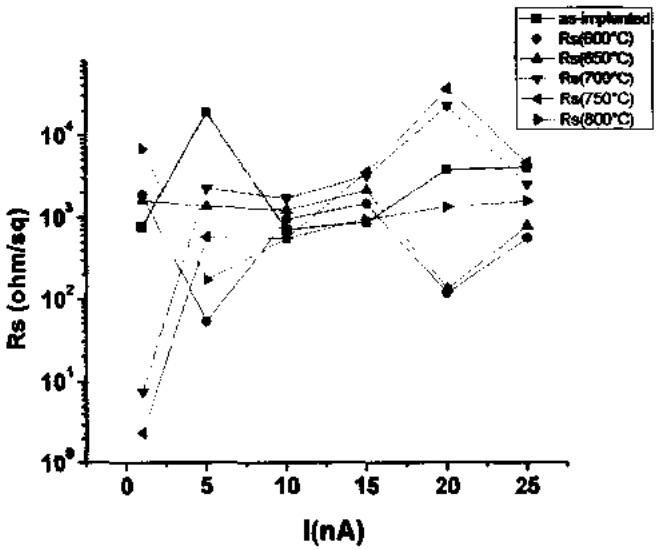


Figure 5.8: Variation of sheet resistance, obtained from Hall Measurement System, for In+C co-implanted n-type silicon substrate against current ranges 1 nA-30 nA at different annealing temperatures. The values plotted here are averaged against the data obtained after repeated measurements for each sample to assure the reliability and tolerance.

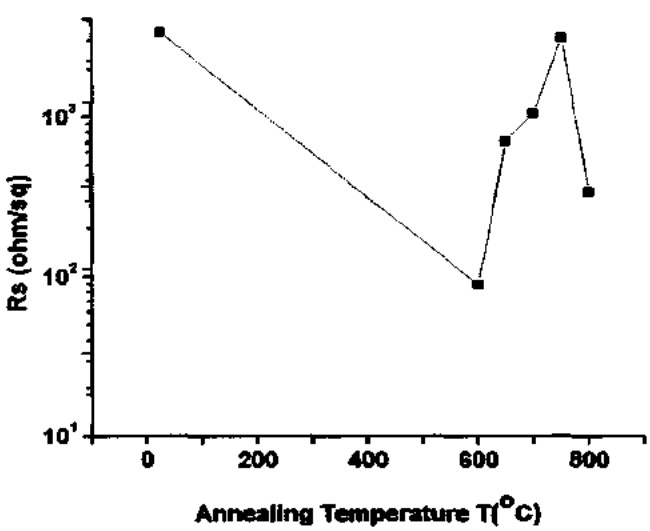


Figure 5.9: Variation of sheet resistance obtained from Keithley 4200 IV/CV system, for In+C co-implanted n-type silicon substrate against post annealing temperatures from 600°C-800°C. The values plotted here are averaged against the data obtained after repeated measurements for each sample to assure the reliability and tolerance.

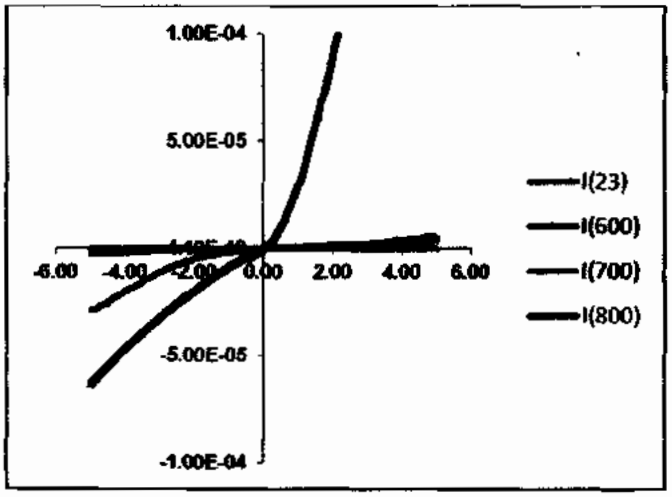


Figure 5.10: Variation of current I(mA) with respect to voltage V(volts), obtained from Keithley 4200 IV/CV system, for In+C co-implanted n-type silicon substrate for annealing temperatures from 600°C-800°C. The values plotted here are averaged against the data obtained after repeated measurements for each sample to assure the reliability and tolerance.

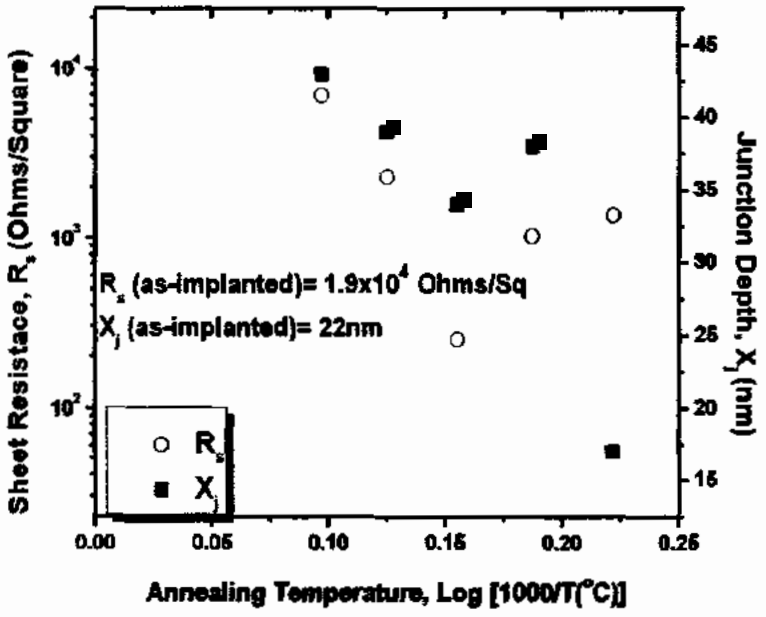


Figure 5.11: Variation of sheet resistance and junction depth (Xj), obtained from Hall Measurement System, Keithley 4200 and CV measurement system for In+C co-implanted n-type silicon substrate against different annealing temperatures. The values plotted here are averaged against the data obtained after repeated measurements by three different techniques for each sample to assure the reliability and tolerance.

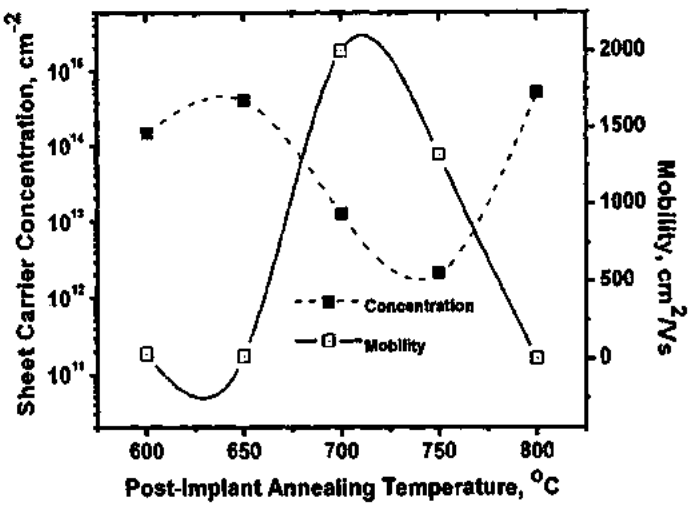


Figure 5.12: Two plots showing variation of retained sheet carrier concentration and carrier mobility with respect to different annealing temperatures for In+C co-implanted n-type Si substrate. Again, the data plotted here are average values obtained by three different techniques on various samples.

5.3 Analysis of Ellipsometric Measurements

Another method used for the measurement of junction depth is Ellipsometry. The thickness of implanted layers were extracted by using one layer model which consists of one standard doped silicon layer on conventional silicon substrate to efficiently focus the measurement on active regions where ultra shallow junctions are stably formed and electrically activated. The measured values from ellipsometer, (ψ) and (Δ) as shown in figures 5.13, 5.14 and 5.15 were directly used to determine absorption coefficient (α), refractive index (n) and effective junction thickness (X_j).

5.3.1 One Layer Model for the Measurements of Thickness

Ellipsometry utilizes polarized light to characterize thin films, surfaces, and material microstructure [120,121]. Light can be polarized in two directions: parallel and perpendicular to the plane of incidence. These are denoted as p-polarized and s-polarized. When the incident beam of light is reflected at a substrate or layer interface,

the change in polarization state of the light reflected from the surface is measured from the complex ratio,ρ of s-polarized and p-polarized reflectances, r the measured values are expressed as Psi (ψ) and delta (Δ) are related to the ratio of Fresnel reflection coefficients, r_p and r_s for p- and s-polarized light, respectively [49].

$$\rho = \frac{rp}{rs} = \tan(\psi) e^{i\Delta} \quad (5.1)$$

In equation 5.1 the angle Δ is the change in phase difference between *p* and *s* polarized light during reflection and ψ is the angle at which the tangent is the ratio of the magnitude of total reflection coefficient. Measurement of values for ψ and Δ at each wavelength gives ellipsometric spectrum. This spectrum when measured at oblique angles of incidence gives extremely sensitive function of a sample. In equation 5.1 *tan* (ψ) gives the amplitude and $e^{i\Delta}$the phase. By using this polarization ratio, ρ the real part of the refractive index, *n* and the imaginary part, called the extinction coefficient, *k* was obtained and used to calculate the absorption coefficient, α [120, 1121, 49].

$$\alpha = \frac{4\pi k}{\lambda} \quad (5.2)$$

5.3.2 Formula Derivation for thickness measurement

For the ultra shallow junction (USJ) on bulk, one layer model is used which consists of one doped silicon layer on un-doped silicon substrate [42]. The total reflection coefficient for the system is:-

$$R = \frac{rp01 + rp12e^{-2i\delta}}{1 + rp01\,rp12e^{-2i\delta}} \quad (5.3)$$

But in Ellipsometry, P and S polarization states were treated independently as:-

$$R_p = \frac{rp01 + rp12e^{-2i\delta}}{1 + rp01\,rp12e^{-2i\delta}} \quad (5.4)$$

$$R_s = \frac{rs01 + rs12e^{-2i\delta}}{1 + rs01\,rs12e^{-2i\delta}} \quad (5.5)$$

The Fresnal reflection coefficients are determined by the following equations:-

$$r_s01 = \frac{rsn1\cos\theta0 - n0\cos\theta1}{n1\cos\theta0 + n0\cos\theta1} \quad (5.6)$$

$$r_s01 = \frac{n0\cos\theta0 - n1\cos\theta1}{n0\cos\theta0 + n1\cos\theta1} \quad (5.7)$$

$$r_p12 = \frac{n2\cos\theta1 - n1\cos\theta2}{n2\cos\theta1 + n1\cos\theta2} \quad (5.8)$$

$$r_s12 = \frac{n2\cos\theta1 - n1\cos\theta2}{n2\cos\theta1 - n1\cos\theta2} \quad (5.9)$$

Where the subscripts 0, 1, and 2 denote the air, junction (indium +carbon co-implanted part of Si) and substrate (silicon) mediums respectively. The total reflection coefficient in the complex phase is:

$$R_p = |R_p|\, e^{i\delta p} \quad (5.10)$$

$$R_s = |R_s|\, e^{i\delta s} \quad (5.11)$$

Where $|R_p|$ and $|R_s|$ represent the amplitude attenuation, and δp and δs represent the phase shifts in the P and S polarization states respectively [49]. By using equations, 5.10 and 5.11, we can easily calculate the angles:-

$$\mathrm{Tan}\Psi = \frac{|Rp|}{|Rs|} \quad (5.12)$$

$$\Delta = \delta p - \delta s \quad (5.13)$$

The complex reflectance ratio becomes:-

$$\rho = \frac{rp}{rs} = \tan(\psi) e^{i\Delta} = \left(\frac{rp01 + rp12 e^{-2i\delta}}{1 + rp01\, rp12 e^{-2i\delta}}\right) x \left(\frac{rs01 + rs12 e^{-2i\delta}}{1 + rs01\, rs12 e^{-2i\delta}}\right) \quad (5.14)$$

The junction thickness was measured by the following equation

$$d = \delta\left(\frac{\lambda}{360}\right)(n_1^2 - \sin^2\phi)^{-1/2} \quad (5.15)$$

5.3.3 Measurement Analysis

The values of Ellipsometric angles as a function of the wavelength for incidence angle 70 degree, was measured for crystalline Silicon after indium plus carbon co-implantation. The results of measurements ψ and Δ are presented in figures 5.13, 5.14 and 5.15. The optical behavior of as-implanted and annealed samples shows that the annealing changes the optical constants of the ion irradiated samples; these changes of the optical constants are in the region 360 nm-730 nm.

The refraction, n and extinction coefficient, k determined for In+C co-implanted n-type substrate are presented in figures 5.16 and 5.17. These figures show that after implantation refractive index decreases in the whole range of studied spectrum. Figure 5.18 shows that by co-implantation of In+C, refractive index gets reduced due to the amorphous layer and defect generation in silicon substrate. As the annealing temperature increased from 600°C-800°C, the process of damage recovery occurs and atoms try to settle down on their proper positions. This, in turn increases the refractive index. Figure 5.19 shows that annealing at different temperatures (600°C, 700°C, 750°C and 800°C tends to increase the refractive index for wavelength in the range 360-920 nm. This shows that uniformity or periodicity exist between these temperature ranges. Figure 5.19 also shows that by increasing temperature refractive index increases because of the variation of refractive index with temperature. This may be due to the thermo optic effect in which the phonons and electrons modify the refractive index at different temperature affecting the interaction of light with the material. Refractive index of material depends on temperature due to two basic properties of the material,

the thermal expansion and the temperature dependence of the energy band gap. Band gap shift due to electron- phonon interactions modify the band structure as the temperature changes [132].

Figures 5.20, 5.21 and 5.22 show the real and imaginary part of the dielectric function for In+C co-implanted n-type silicon substrate at different annealing temperatures. The dielectric function of indium+carbon co-implanted Si-substrate exhibit a significant reduction with respect to bulk crystalline silicon, which is attributed to the quantum size effect. It is also observed that after annealing from 600°C-750°C dielectric constant increases due to the intrinsic property of indium at 800°C. As temperature increases, the molecules in the dielectric have more thermal energy and therefore, the amplitude of random motion is greater. This means that the molecules are less closely aligned with each other. Hence, the dielectric constant reduces.

Figure 5.23 further shows the absorption coefficient for Si substrate, as implanted and annealed samples with respect to various wavelengths. It is evident that the shorter wavelengths give higher absorption coefficient and higher sensitivity at lower wavelengths, but a drastic decrease of absorption coefficient is observed at higher wavelengths. After In+C co-implantation, it may be noticed that without having any extra ordinary variation in the behavior, the absorption coefficient, α is almost maintained in the whole range of studied spectrum and this behavior also maintained after annealing at temperature ranging from 600°C-800°C. These, however, is lower than the value of α for as-implanted samples. indium absorption coefficient at 600°C decreases more than those at 750°C because of the behavioral difference of Indium at 600°C-650°C. Absorption coefficient at 800°C (and possibly above) withstands the trend and decreases due to possible free carrier absorption dominan-ce in this range. For getting best performance of ultra-shallow junctions in CMOS and consequent efficient operational parameters such as response time and higher speed, absorption coefficient should be high [134], which describe that the larger number of photons should be absorbed in the depletion regions of the device. The relative depth to which photons penetrate is a function of its wavelength, but absorption would change as a function of time as the implant damages were annealed out. It also shows that initially

the wafer was pseudo-amorphous (as implanted) so its absorption was high and reflectivity was low, but absorption changed as a function of time as the samples were annealed out. Figure 5.23 show that by using this recipe, we have obtained a window of almost constant absorption coefficient between the range 400 nm-900 nm at annealing regime 600°C-800°C. We are working in this domain because the sensitivity range of wavelength in CMOS technology is between 400-850 nm. For larger wavelengths λ>950 nm, photon energy is not high enough to create an electron-hole pair and no electrical signal can be detected. For lower wavelengths, λ<400 nm, excess carriers are generated very close to the surface, surface recombination rate becomes high and only a small part of them can contribute to the photocurrent [139, 140, 141]. By using expression 5.15, junction depth calculated which was in the range of 9 nm-60 nm as shown in figure 5.24.

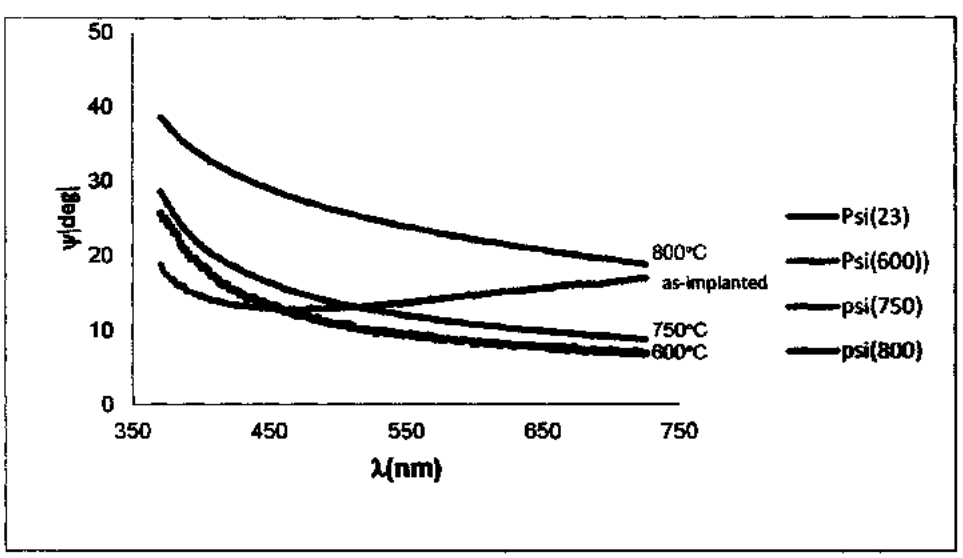


Figure 5.13: Ellipsometric Psi (ψ) spectra at 70 angle of incidence for as-implanted and RTA annealed In+C co-implanted Si substrate.

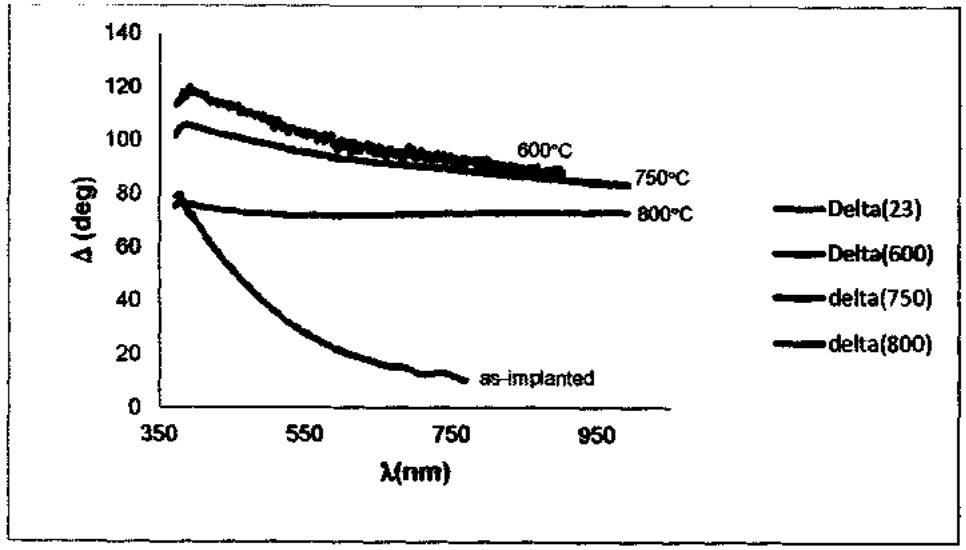


Figure 5.14: Ellipsometric delta (Δ) spectra for 70° angle of incidence for RTA annealed In+C co-implanted Si substrate.

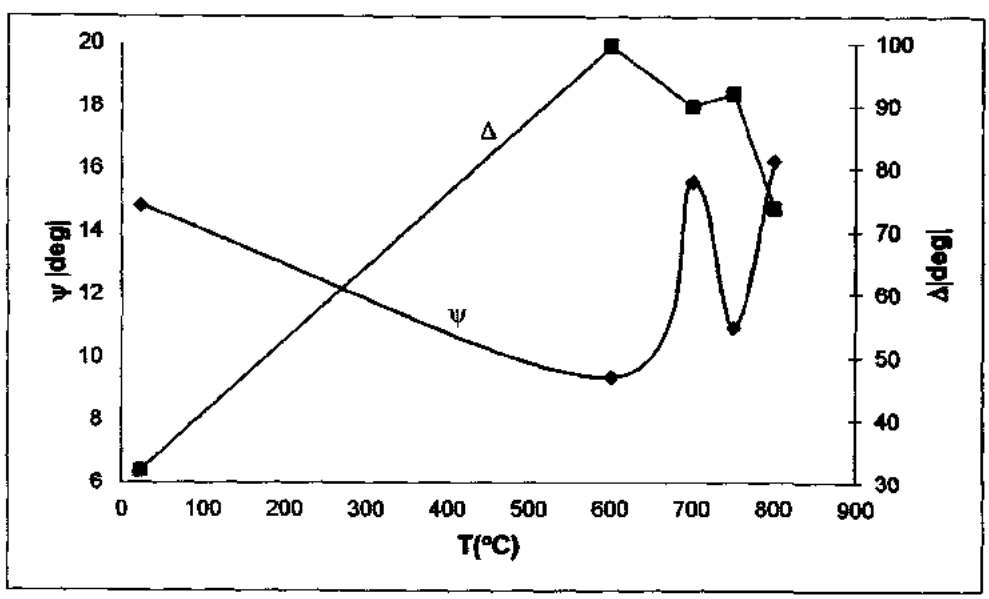


Figure 5.15: Effect of temperature on Ellipsometric Psi (ψ) spectra and Ellipsometric delta (Δ) spectra at 70° angle of incidence for RTA annealed In+C co-implanted Si substrate.

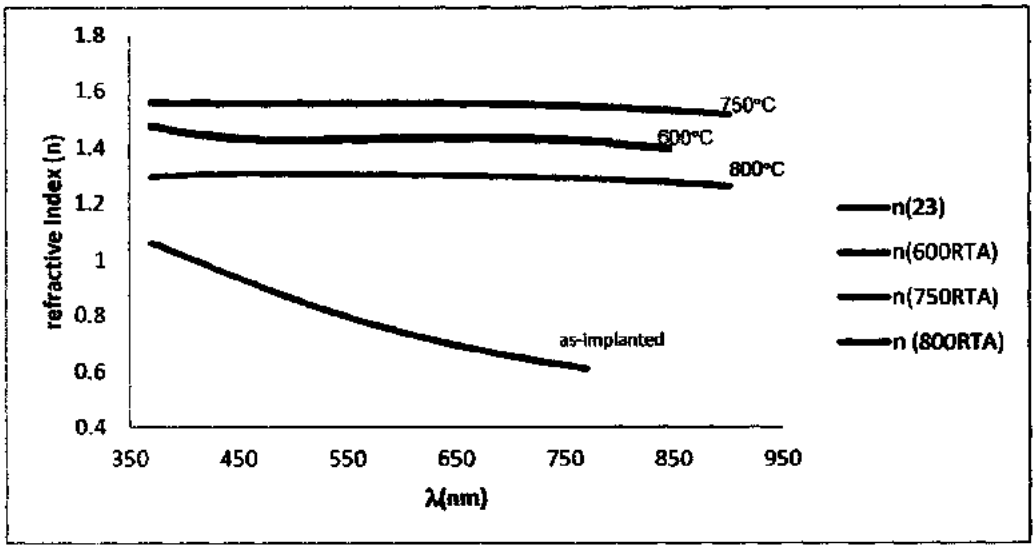


Figure 5.16: Refractive index versus wavelength, this figure shows the variation of refractive index with respect to wavelength at different temperature. The data shows that uniformity or periodicity exist between these temperature ranges.

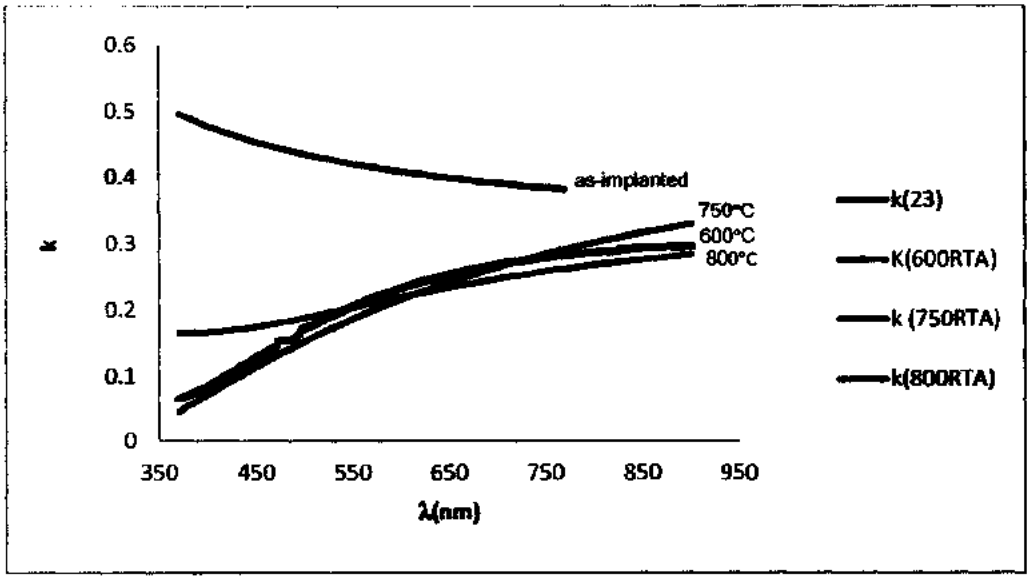


Figure 5.17: This figure shows the variation of imaginary part of refractive index with respect to wavelength for both as implanted and annealed In+C co-implanted Si-substrate.

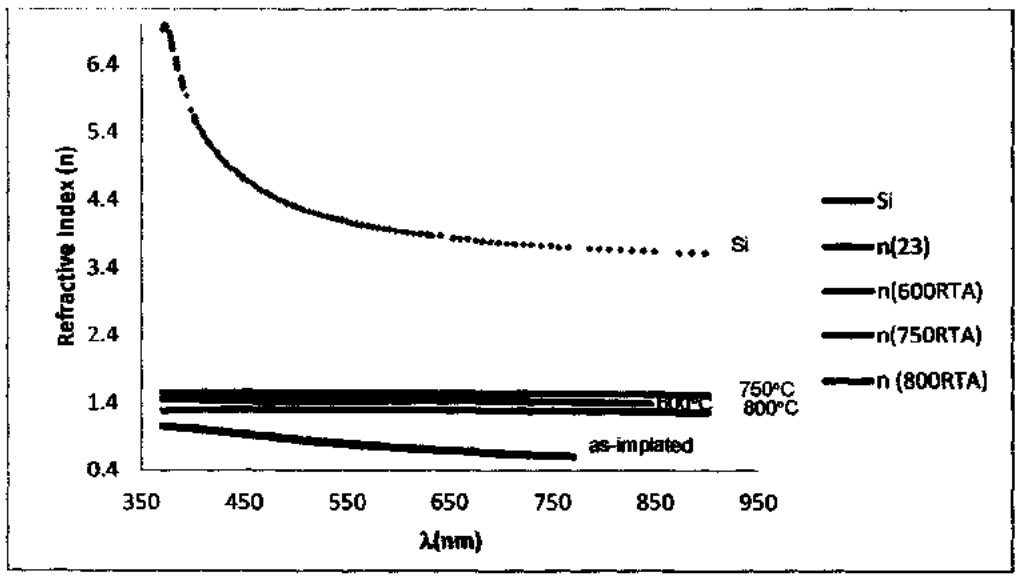


Figure 5.18: This figure shows the variation of real part of refractive index with respect to wavelength for both as implanted and annealed In+C co-implanted Si-substrate.

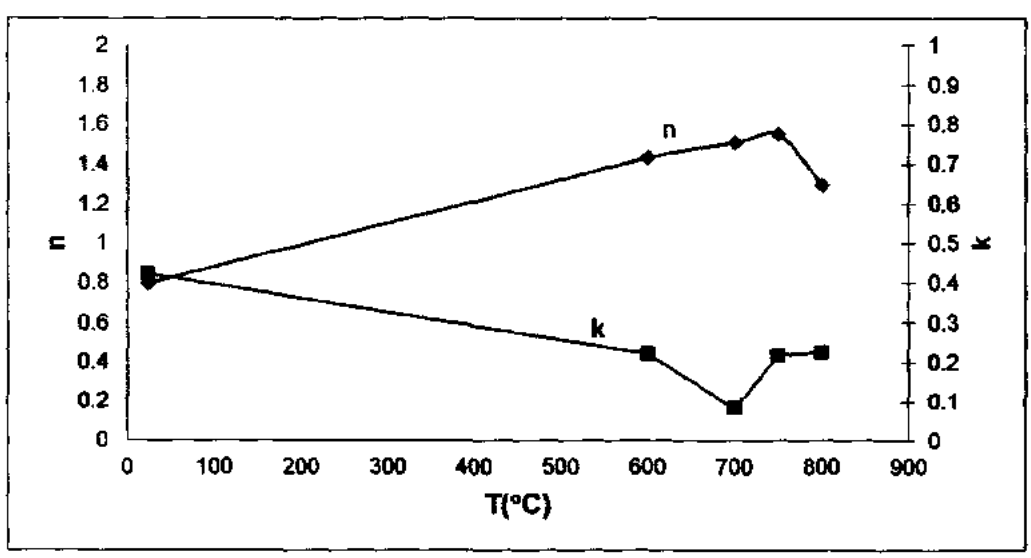


Figure 5.19: Ellipsometric spectra at 70° angle of incidence for both as-implanted and RTA annealed In+C co-implanted Si substrate. Average values of n and k are taken at different annealing temperatures.

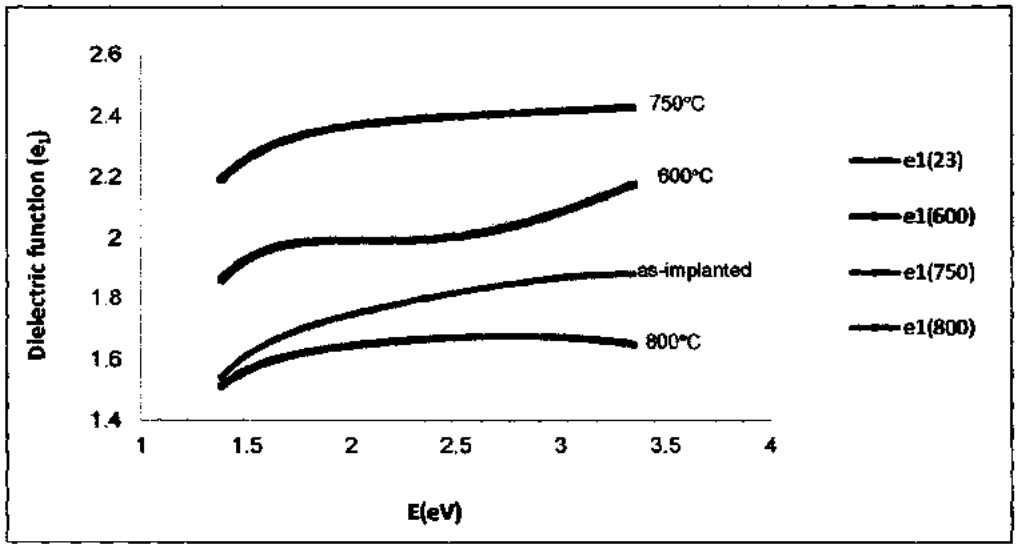


Figure 5.20: Real part of the dielectric function for In+C co-implanted n-type silicon substrate at different annealing temperatures.

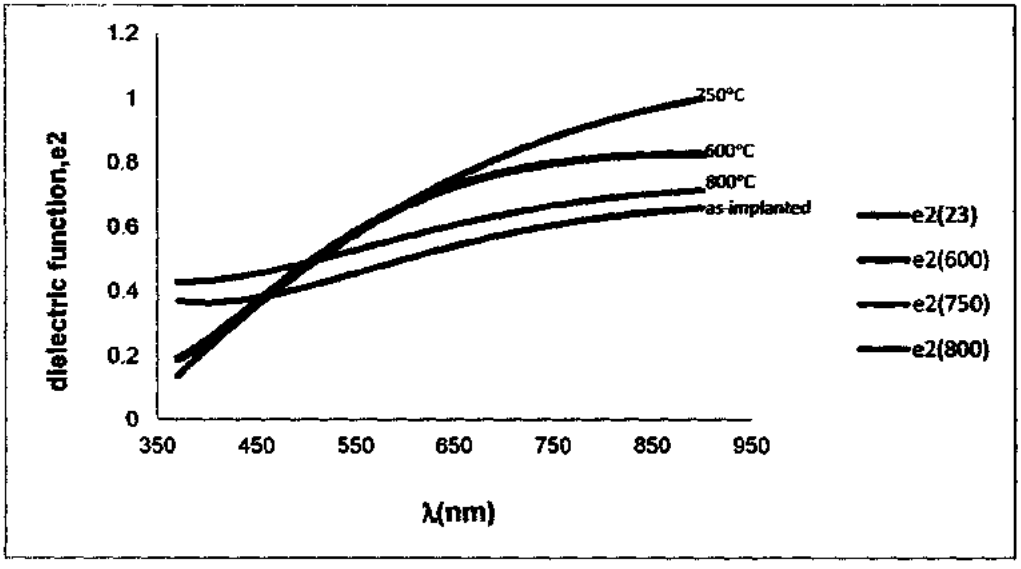


Figure 5.21: Imaginary part of the dielectric function for In+C co-implanted n-type silicon substrate at different annealing temperatures.

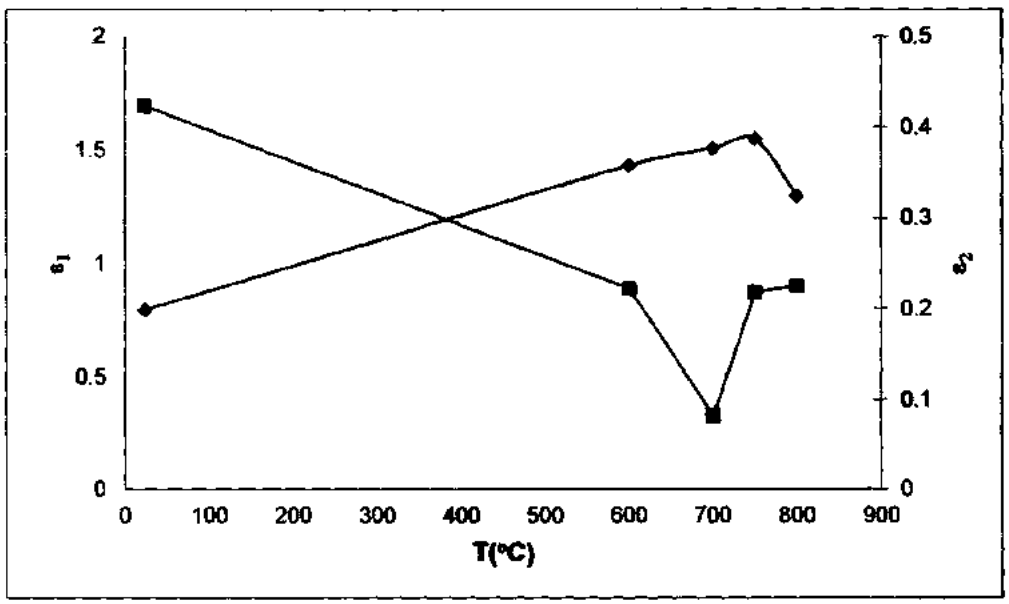


Figure 5.22: Effect of annealing temperature on real part (ε_1) and imaginary parts (ε_2) of In+C co-implanted n-type silicon substrate.

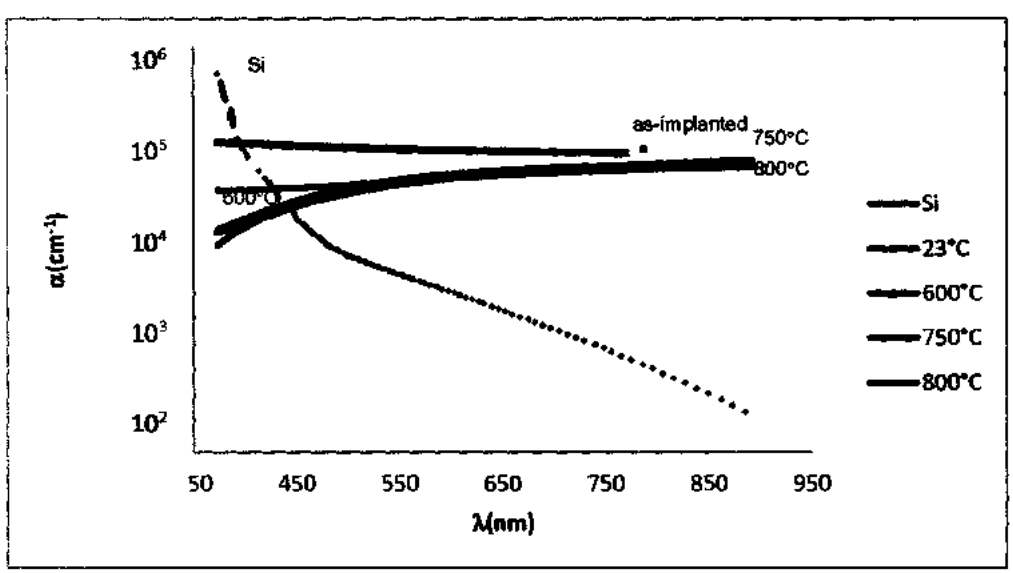


Figure 5.23: The figure shows the variation of absorption coefficient with respect to wavelength for silicon, as-implanted In+C co-implanted n-type silicon and annealed In+C co-implanted silicon substrate.

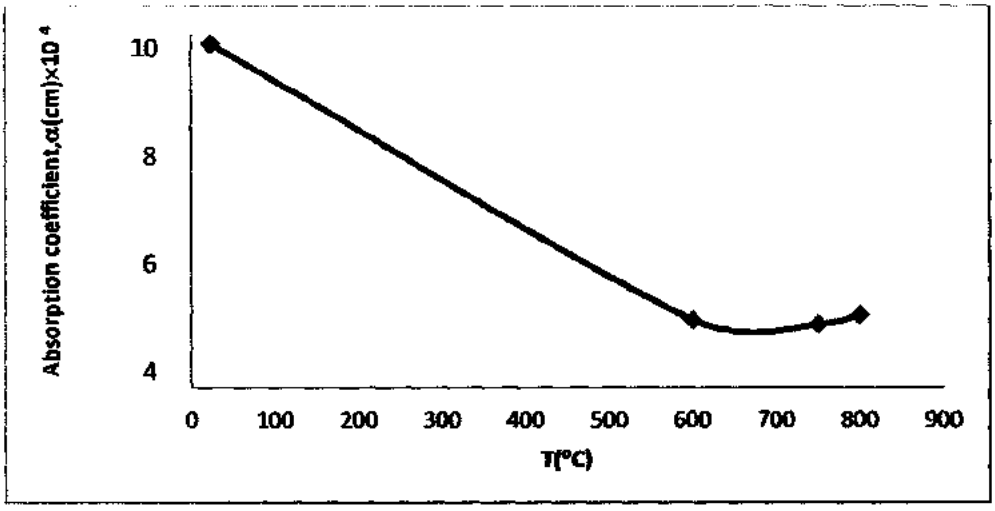


Figure 5.24: Effect of annealing temperature on absorption coefficient.

5.4 Analysis of RBS Results

Energy of scattered protons or Helium ion gives light element composition and elemental depth profiles in Rutherford Backscattering Spectroscopy (RBS). RBS is very useful technique for the qualification of ultra shallow junction (USJ) samples. RBS has become a regular testing technique in the running fabrication plants for indirect investigation of thickness and atomic distribution (FABs) where CMOS transistors with decreasing scaling of junction depth are manufactured because RBS with and without channeling offers independent method of measuring the range profile, location of impurities, implantation dose and damages due to implantation. Keeping this very fact in mind, samples were tested against RBS protocols. The light dopant composition and depth profiles obtained by RBS technique were studied together with the similar profiles obtained by Electrical measurements.

Figure 5.25-5.32 Shows a spectrum for He^{++} ions backscattered at an angle of 170° from the active region of In+C co-implanted p-type Si samples of as implanted and annealed at different annealing temperatures from 600°C-800°C. Indium peaks were detected at 2.085 MeV, while carbon peaks were detected at 4.267 MeV. These spectra were used to calculate the junction depths in as-implanted and annealed In+C

co-implanted n-type silicon substrates. Thickness of the active region for as implanted and post annealed In+C co-implanted n-type Si samples were deduced as shown in Table 5.1. Figures 5.25-5.32 shows an energy spectrum of 2.088 MeV He ion backscattered from a Si target with In+C at 70 keV and 10 keV with doses 5.7×10^{14} In(at/cm^2) and 3.4×10^{15} C(at)/cm^2). The silicon signal gives a step with leading edge at 1.13 MeV and the indium signal has a Gaussian distribution with a peak at 1.8 MeV and the carbon signal has a Gaussian distribution shows an energy spectrum of 4.267 MeV. The shift in energy (ΔE_{In}) and full width at half maximum (FWHM) of indium peak for as-implanted and annealed samples as calculated from RBS spectrum are shown in Table 5.1. It is assumed that indium is so shallow that the surface energy approximation can be used in calculating the stopping cross section. The maximum concentration of indium in silicon is estimated from the peak height of the indium signal. To obtain concentration profile stopping cross-section factor was used, which gives energy to depth conversion for scattering of indium in silicon matrix as in equation.5.16. For this purpose the formula derived for the bulk impurities is shown in equation. 5.17.

$$N_{In} = \frac{H_{In}}{H_{Si}} \frac{\sigma_{Si}}{\sigma_{In}} \frac{[\varepsilon_0]_{In}^{Si}}{[\varepsilon_0]_{Si}^{Si}} N_{Si} = \text{at. \%} \qquad (5.16)$$

$$N_{si} R_p = \frac{\Delta E}{[\varepsilon_0]_{In}}{}_{Si} = 0.201\times10^{18} \qquad (5.17)$$

$N_{Si}=4.98\times10^{22}$ at/cm^3, Rp is the projected range of the implanted indium. By putting value of N_{Si} in equation 5.17 we obtain Rp=40 nm. As we know that the implant distribution is Gaussian so depth of indium will be its projected range. The projected range, dopant percent concentration, junction depth and junction thickness calculated for In+C co-implanted silicon substrate for as-implanted and annealed samples is given in Table 5.1 and in figures 5.33, 5.34 and 5.35. The results further suggests that the stability of shape, abruptness of the junction and the dopant profile activated under a certain thermal condition is grossly dependent on a carefully chosen time–temperature annealing cycle and the physical behavior of the dopants implanted in the junction

matrix. The quality, shape and profile of the ultra shallow junction as exhibited by electro-optical parameters in this study may have ramifications for device engineers while fabricating CMOS on sub 10 nm technology nodes.

Table 5.1: Shows the results obtained from RBS measurements.

T(°C)	Energy shift (keV)	FWHM (nm)	Rp (nm)	In+C layer thickness (nm)	In+C layer depth (nm)	% Conc. Si	% Conc. In	%Conc. C
As-implated	21.30	13	40.4	13	41	0.375	1.3	0.52
600	6	14	12.1	11	10	0.36	1	0.5
650	23	10	46.4	8	44	0.335	1	0.5
700	19	9	38.3	10	42	0.325	0.85	0.48
750	21.5	10	43.4	9	40	0.32	0.82	0.47
800	20.5	10	41.4	14	39	0.315	0.8	0.5

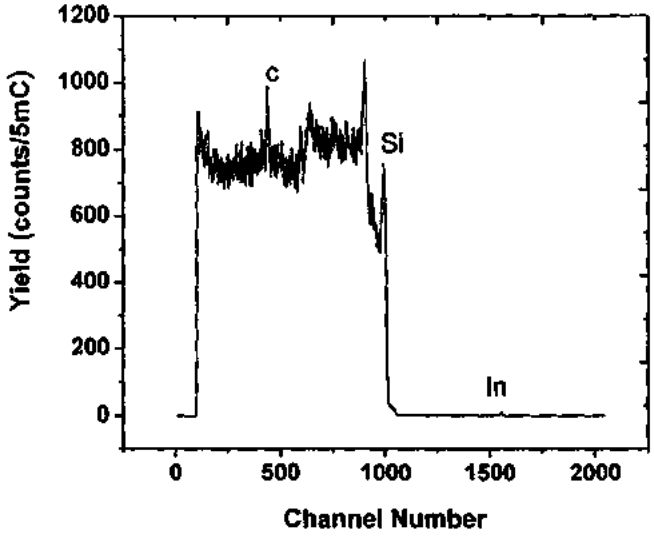


Figure 5.25: Rutherford Back Scattering Spectrum recorded for He^{++} ions of energy 2.085 MeV incident on the In+C co-implanted n-type Si substrate showing results of RBS yields of as implant. The C, Si and In peaks are also identified.

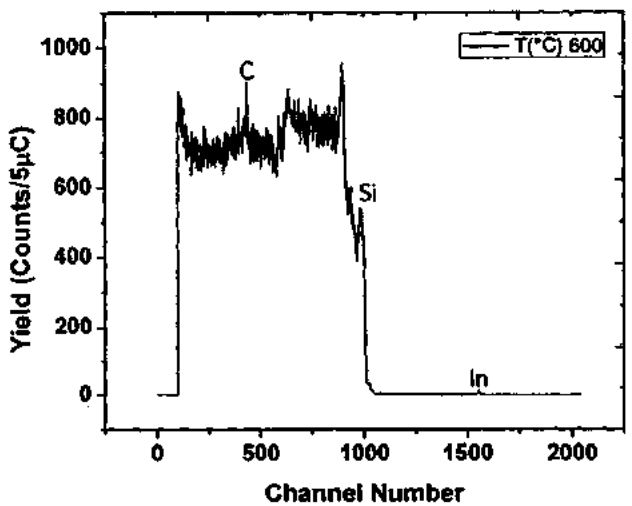


Figure 5.26: RBS spectrum recorded for He^{++} ions incident on the In+C co-implanted n-type Si substrate showing results of RBS yields of samples annealed at 600°C. The C, Si and In peaks are also identified.

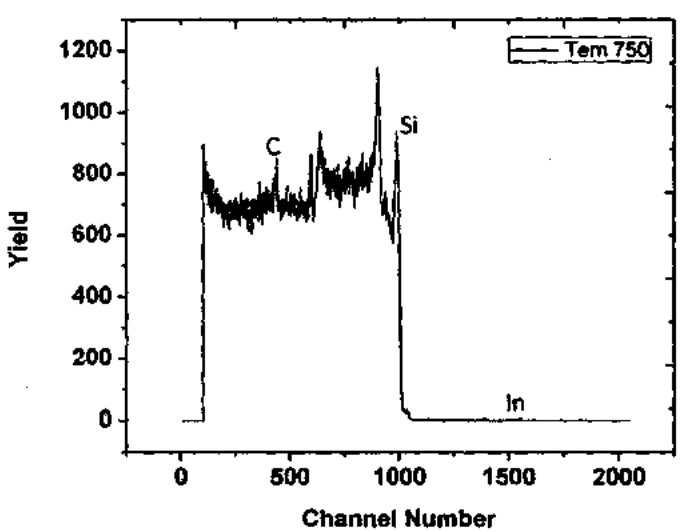


Figure 5.27: RBS spectrum recorded for He^{++} ions incident on the In+C co-implanted n-type Si substrate showing results of RBS yields of samples annealed at 750°C. The C, Si and In peaks are also identified.

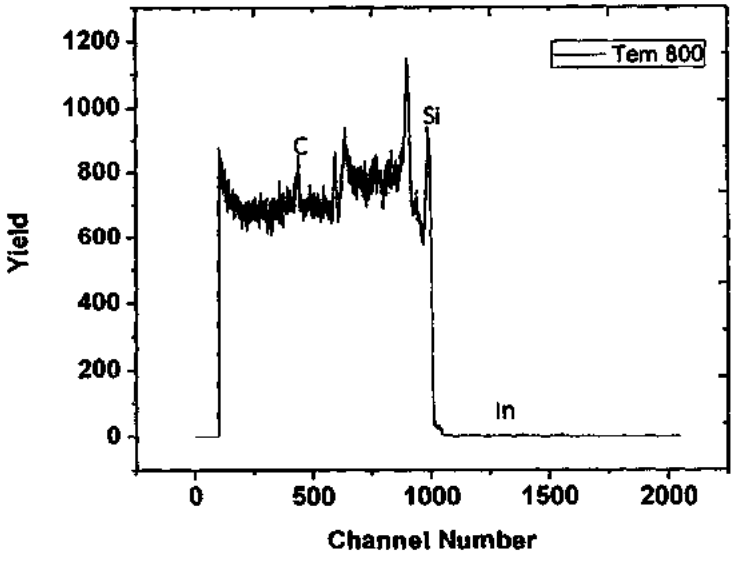


Figure 5.28: RBS spectrum recorded for He^{++} ions incident on the In+C co-implanted n-type Si substrate showing results of RBS yields of samples annealed at 800°C. The C, Si and In peaks are also identified.

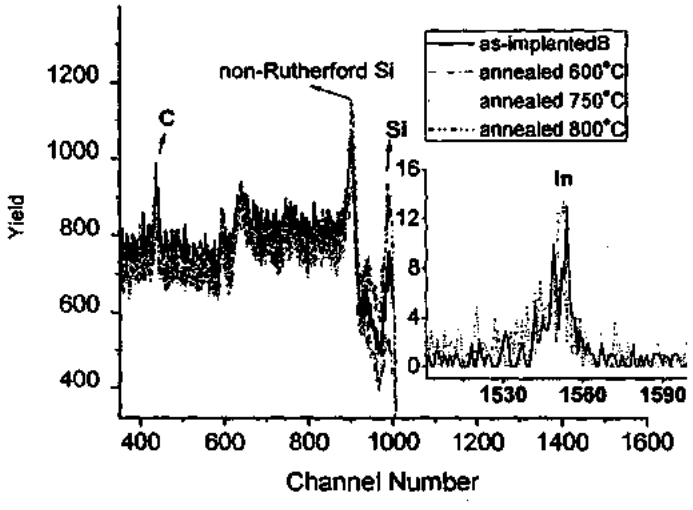


Figure 5.29: RBS spectrum recorded for He^{++} ions incident on the In+C co-implanted n-type Si substrate showing a comparison of as implanted and annealed (600°C-800°C) results of RBS yields. The C, Si and In peaks are also identified.

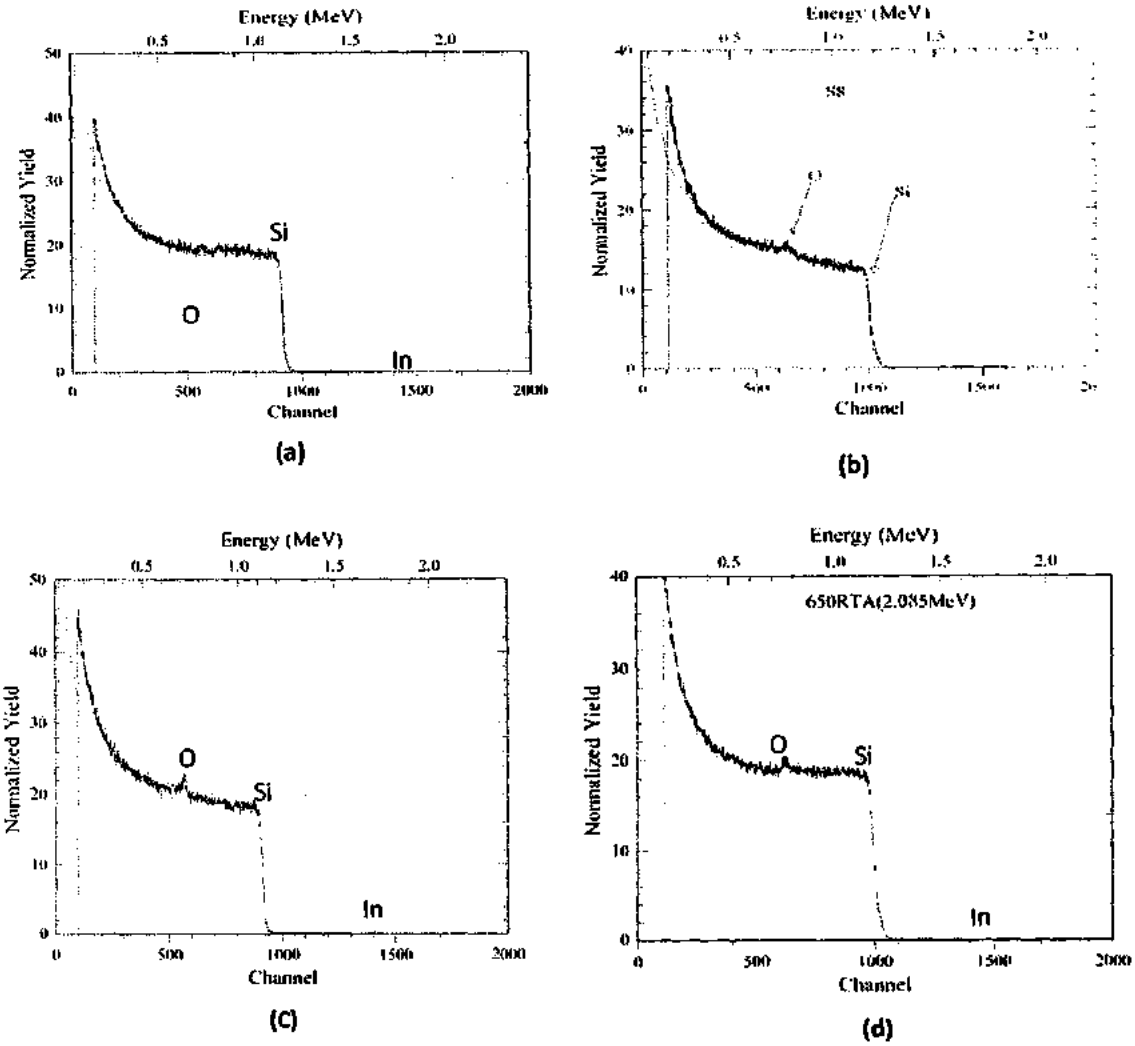


Figure 5.30: RBS spectrum recorded for He^{++} ions (2.085 MeV) incident on the In+C co-implanted n-type Si substrate showing a comparison of as implanted and annealed results of RBS yields. The C, Si and In peaks are also identified. (a) and (b) RBS Spectrum of as-implanted In+C co-implanted silicon substrate (C) In+C co-implanted Si substrate post annealed at 600°C for 60 sec (d) In+C co-implanted Si substrate post annealed at 650°C for 60 sec.

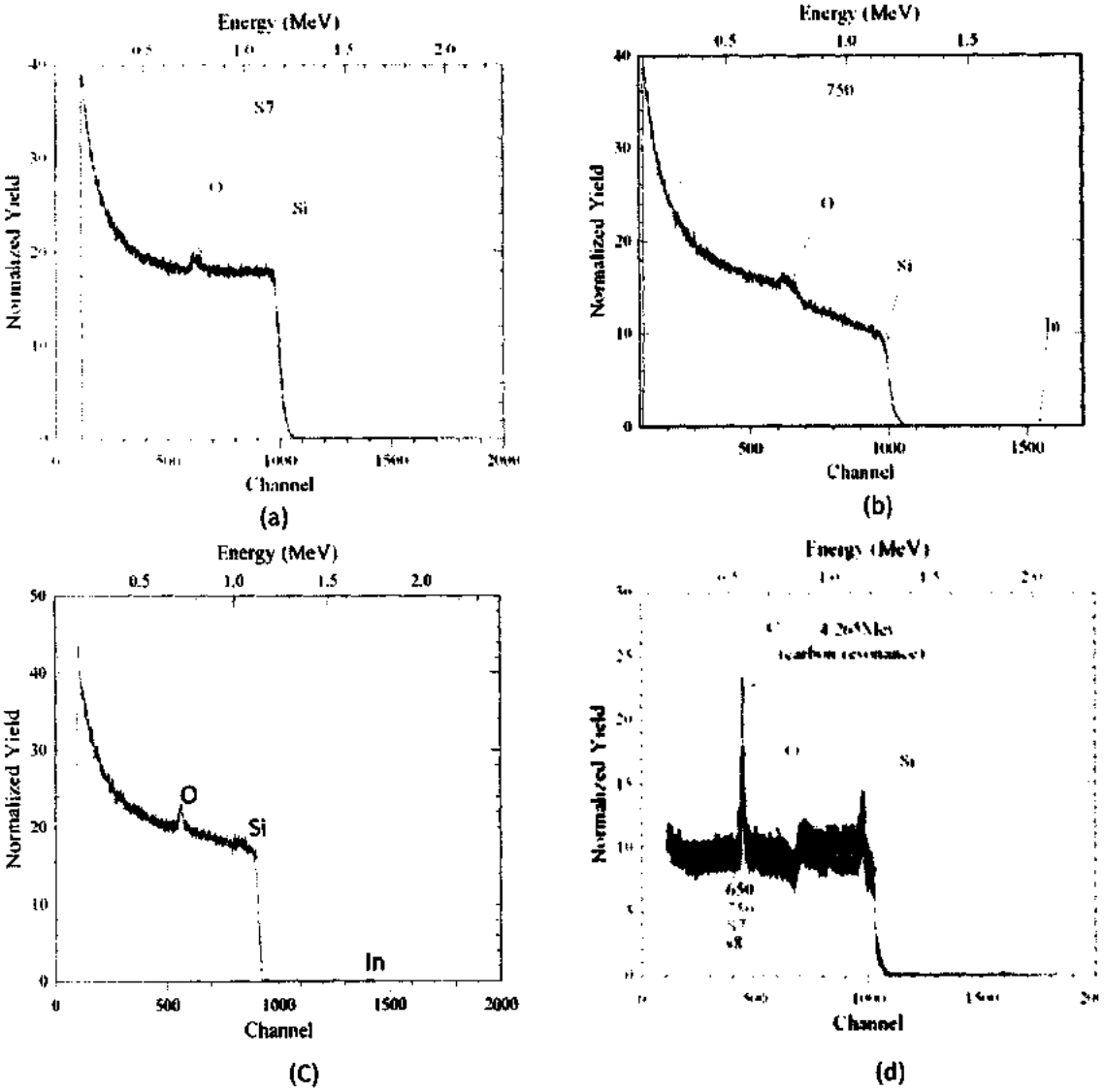


Figure 5.31: RBS spectrum recorded for He^{++} ions incident on the In+C co-implanted n-type Si substrate showing a comparison of as implanted and annealed results of RBS yields. The C, Si and In peaks are also identified. In+C co-implanted in Si substrate annealed at (a) 700°C for 60 sec. (b) 750°C for 60 sec. (C) 800°C for 60 sec (d) In+C co-implanted Si substrate for un-annealed and post annealed at 600, 650 and 750°C for 60 sec at 4.26 MeV He^{++} beam energy.

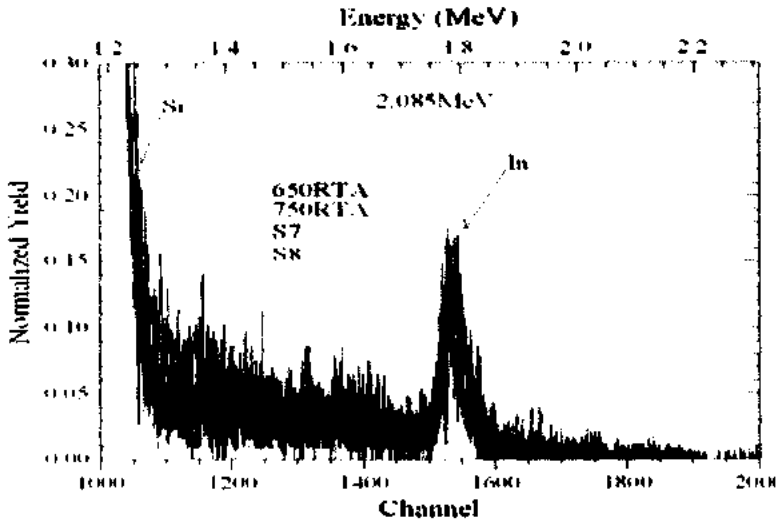


Figure 5.32: RBS spectrum recorded for He^{++} ions incident on the In+C co-implanted n-type Si substrate showing a comparison of as implanted and annealed (600,750 and 800°C) results of RBS yields for indium (In) peaks.

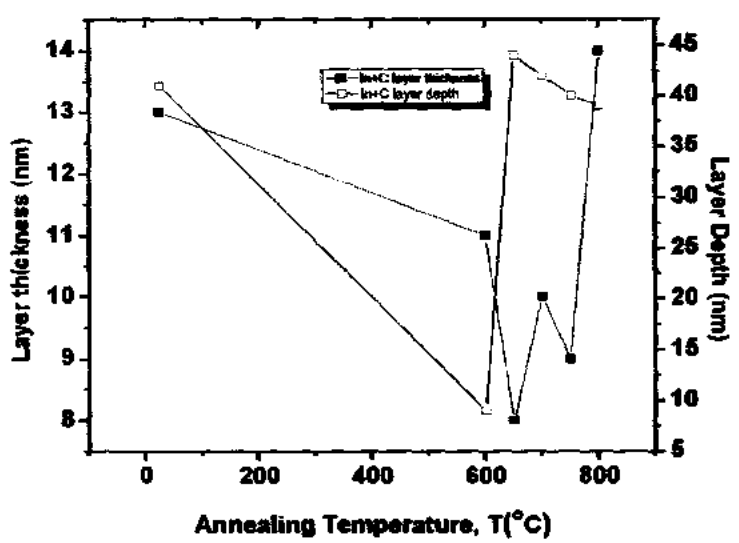


Figure 5.33: Variation of ultra-shallow junction layer thickness and layer depth in substrate with respect to annealing temperature. Results obtained from Rutherford Back Scattering Spectrometry for In+C co-implanted n-type Si substrate.

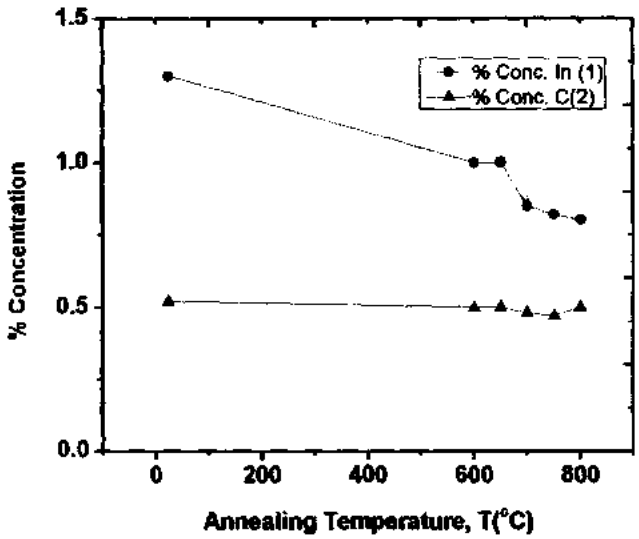


Figure 5.34: % Variation of dopant concentration of indium and carbon with respect to annealing temperature for In+C co-implanted n-type Si substrate.

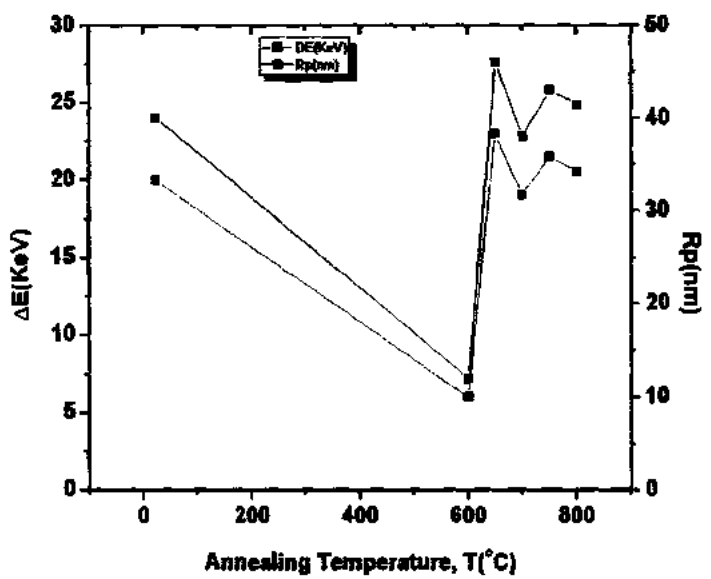


Figure 5.35: Variation of projected range (Rp) and shift in energy (ΔE) with respect to annealing temperature for In+C co-implanted n-type Si substrate.

5.5 Results and Discussion of X-Ray Diffraction

The aim of this characterization is to present the effect of temperature on structural morphology in which effect of temperature on strain is investigated because Strain engineering in semiconductor nano-scale and quantum structures is a powerful strategy to develop novel or improved functionalities [136,137,138]. In particular, the strain influence on the silicon band gap has been exploited to implement higher performance transistors in the current technology [136].

To identify the structure and phase, the diffraction patterns of as implanted and annealed samples of In+C co-implanted Si-substrate were taken. The peaks at 32.95° and 39.178° are assigned to indium (111) and (110) diffractions, respectively. The peak at 42.9° and 44.5° are assigned to carbon (100) and (101) diffractions, respectively. It should be noted that the peak intensities in these figures differ significantly as the annealing temperature is increased. The XRD spectrum in figure 5.36 and 5.37 basically shows the presence of In, C and Si also shown in Table 5.2. In as-implanted samples the Si(400) has maximum relative intensity at 69.129°, when sample is post annealed at 600°C the maximum relative intensity of the peak becomes 14 and a sharp peak appears as a small "hump" but at the same time relative intensity of In(110) at 39.178 change from 0.01 to 15.82. Because due to intrinsic property of indium at 600°C activation of indium atoms increases, due to which intensity of indium increase and the intensity of Si(400) in the figure 5.38 becomes much lower than figure 5.37. The previously sharp Si(400) peak has also broadened, indicating damage to the single crystal as shown in figures 5.38-5.41. Incorporation of dopants (indium and carbon) into a Si layer can contract or expand the lattice of the layer relative to the un-doped Si substrate depending on the covalent bonding radius of the impurity [54]. Hence most of the electrically activated indium atoms reside near the substitutional lattice sites by forming the In–C acceptor centers. The formation of this defect pair should be energetically favored the stresses introduced by implantation due to indium and carbon. Vacancies will interact with substitutional Indium atoms to relax the strain field introduced by the larger covalent radius of In ~0.144 nm! compared to that of Si ~0.117 nm [135]. Figure 5.42 shows the variation of strain and junction depth with respect to

annealing temperature. In which the magnitude of the strain is calculated using Bragg's law relates the inter planer spacing d_{hkl} for Miller indices h, k and l toθ, which is the angle between the incident beam and the lattice planes as in equation [54].

$$n\lambda=2d_{hkl}\sin(\theta) \qquad (5.18)$$

Where 'n, is an integer associated with the order of Bragg reflection and, λ, is the wavelength of the CuKα_1 radiation. The behavior of samples implanted with In and C during RTA is studied. When the samples are RTA post annealed at 600°C junction depth becomes 9-14 nm and strain due to indium atoms increased becomes 0.567% means mobility increases, but by increasing temperature from 600°C to 700°C a drastic decrease in strain due to indium atoms occur, but strain due to carbon atoms and self-interstitials increases as shown in figure 5.42. From 600°C to 700°C Junction depth increase and this increase in junction depth may be attributed to the movement of indium atoms back to their original positions. Interestingly, a slightly different behavior of physical processing at atomistic level is observed when samples were annealed at 750°C. The signature of this process emerges in the form of increase in lattice strain and hence the junction depth decreases. The breaking of C-In complexes may be responsible for this structural activity.

With the further increasing temperature from 750°C-800°C as shown in figure 5.42 a drastic decrease in strain and increase in junction depth occurs. Which shows that damage related strain disappears at temperature round about 750°C. Ion related strain will be present which can be removed by further annealing. At 800°C, the ion-implantation-induced strain in the lattice seems to decrease. Ion related strain is known to be removed almost fully by high temperature annealing in Si. The implantation induced strain in the lattice and activated Indium atoms present near the substitutional lattice sites (and hence forming the C-In acceptor centers) and their subsequent physical behavior while undergoing the post-implant annealing schedules play an important role in making the doped Si layers either relaxed or strained directly impacting the fabrication yield and efficiency of piezoresistors integrated with the Microsystems. There are certain evidences that the vacancies also interact with substitutional indium

atoms to relax the strain field duly introduced by the relatively larger covalent radius of In ~0.144 nm compared to that of Si ~0.11 nm [82]. Also, it has also been observed that the dopants (indium and carbon in this case) in Si may be responsible to make the lattice contracted or expanded depending on the host impurity covalent bond radii [54]. Results summarized in figure 5.42 also augment these findings where strain caused due to co-implantation in Si layers vary with increasing annealing temperature and consequently impact the depth of the junction formed.

In summary, it was studied that the thermal effects on structural and morphological properties of the layers engineered by co-implantation technology in Si, provide a controlled, reliable, repeatable and easy-to drive process to fabricate ultra-thin piezoresistors and ultra-shallow junctions for CMOS compatible fully integrated systems. This study suggests that a careful design of implant-annealing processes may provide a useful process control directly impacting the physical activity at atomistic level such as defect clustering, defect migration and annihilation, movement of dopant atoms within the atom distribution profiles, surface roughness, lattice relaxation and strain duly controllable by the residual thermal flux during the annealing process.

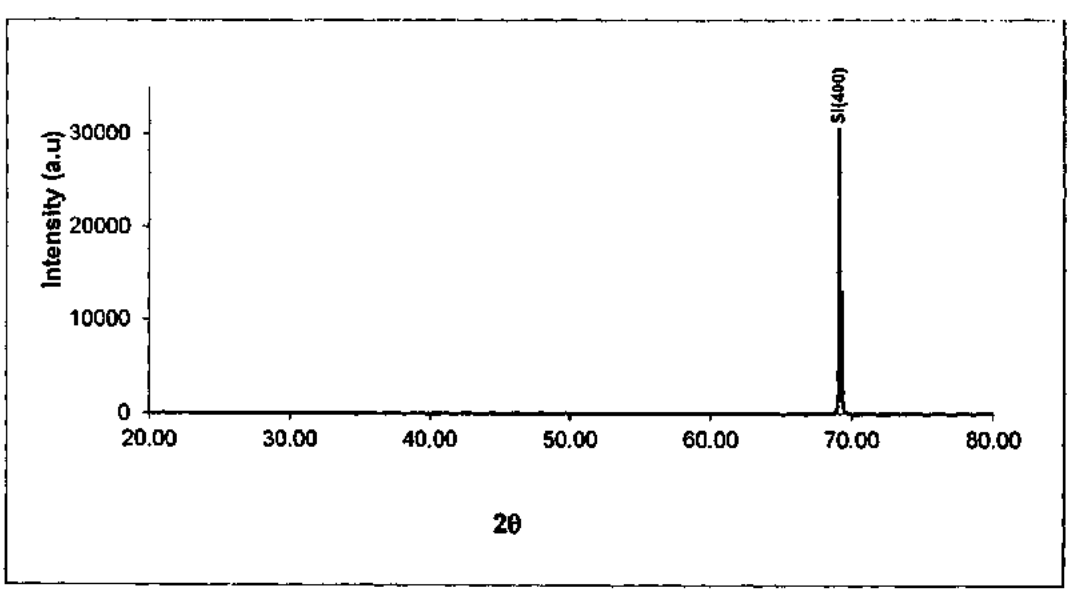


Figure 5.36: XRD Spectrum of as-implanted In+C co-implanted n-type Si substrate.

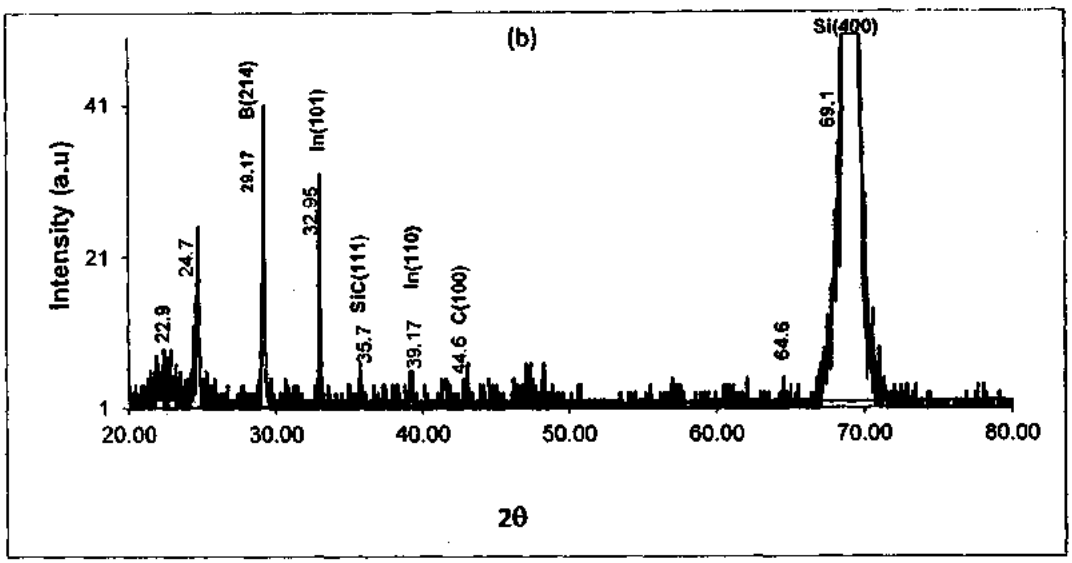


Figure 5.37: XRD Spectrum of as-implanted In+C co-implanted n-type Si substrate at high resolution.

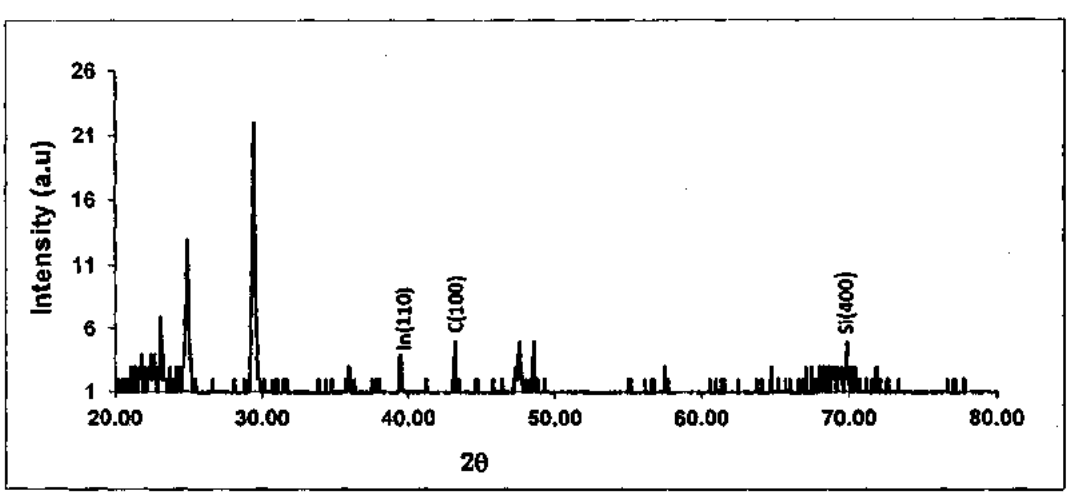


Figure 5.38: XRD Spectrum of In+C co-implanted n-type Si substrate. RTA post annealed at 600°C.

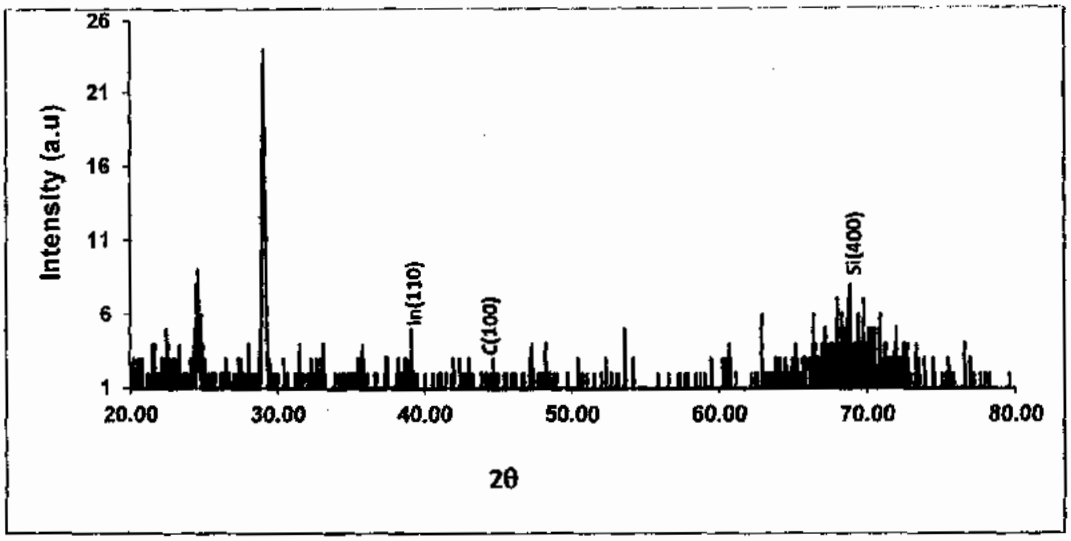


Figure 5.39: XRD Spectrum of In+C co-implanted n-type Si substrate. RTA post annealed at 700°C.

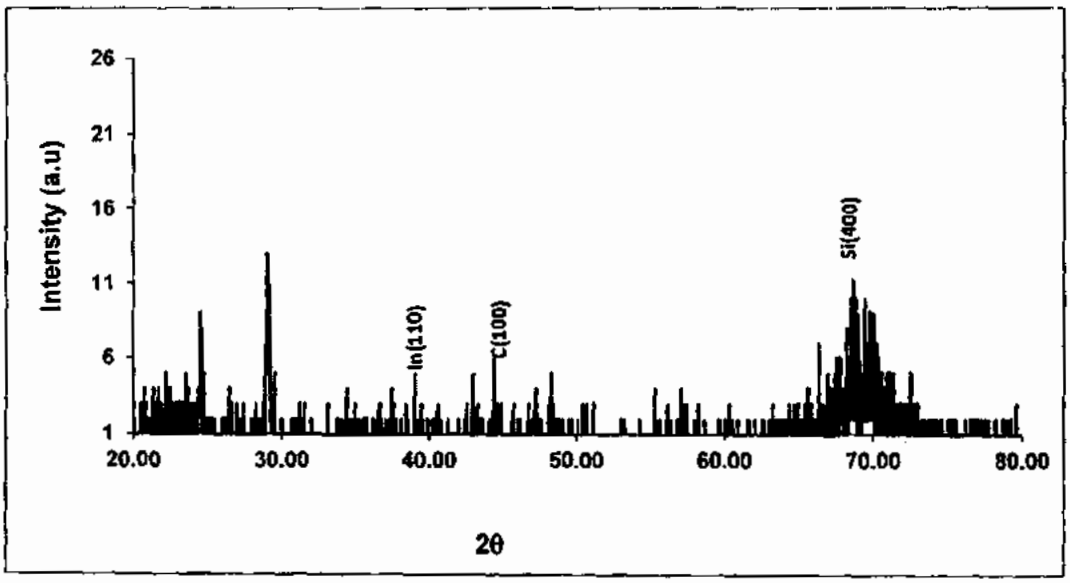


Figure 5.40: XRD Spectrum of In+C co-implanted n-type Si substrate. RTA post annealed at 750°C.

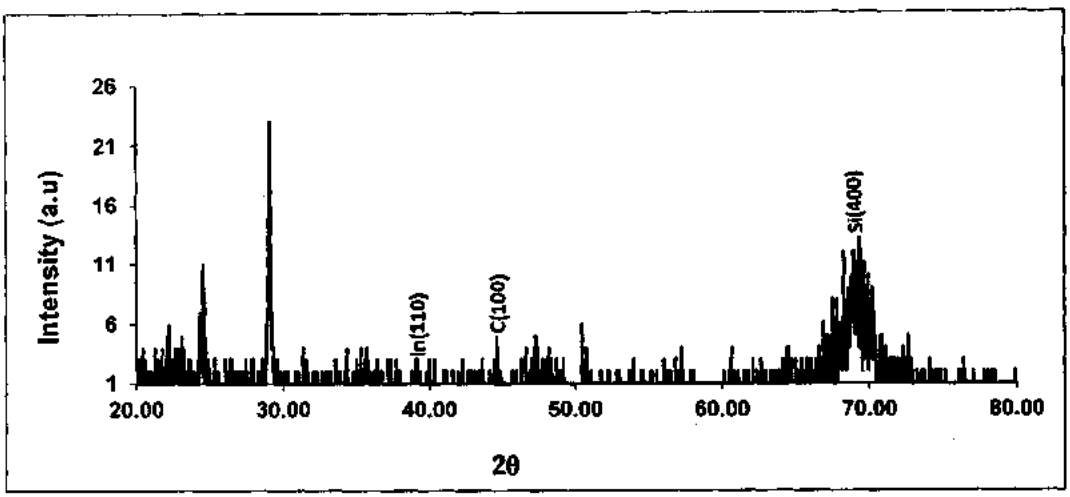


Figure 5.41: XRD Spectrum of In+C co-implanted n-type Si substrate. RTA post annealed at 800°C.

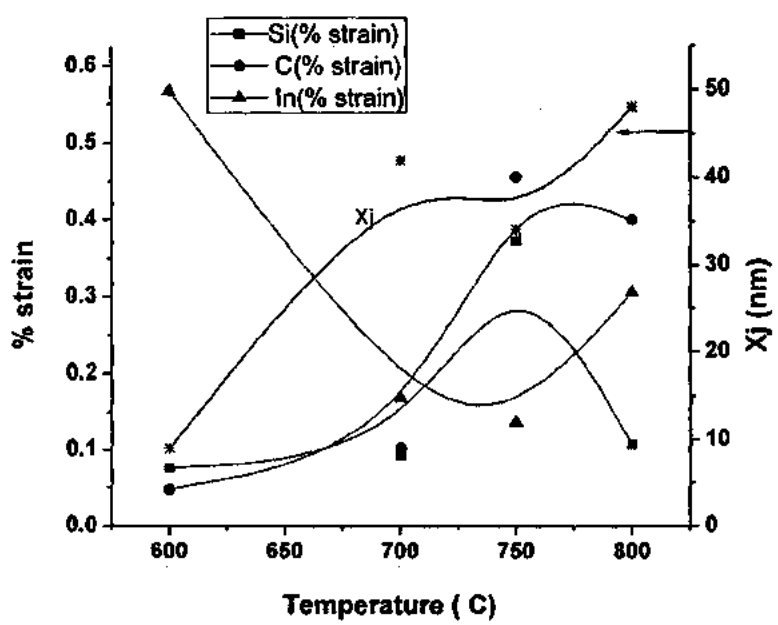


Figure 5.42: Variation of percent change in strain obtained from XRD(X,Pert) as a result of In+C co-implantation in n-type Si (100) substrate with respect to annealing temperature ranging from 600°C to 800°C. and junction depth obtained from different techniques produced previously are also plotted to co-relate the results.

CHAPTER 5 RESULTS, DISCUSSION AND ANALYSIS

Table 5.2: Shows d-spacing and Intensities of elements in In+C co-implanted Si substrate.

As-implanted	θ=24.6578 d=3.61056 ——— Irel=0.04	θ =25.1783 d=3.06065 B(214) Irel=0.13	θ=32.954 d=2.718 In(113) Irel=0.06	θ=35.735 d=2.813 SiC(111) Irel=0.01	θ=39.178 d=2.299 In(110) Irel=0.01 Figure 4.10	θ=42.9165 d=2.1074 C(100) Irel=0.01	θ=47.3252 d=1.92469 Si(220) Irel=0.03	θ =48.278 d=1.88514 B(312) Irel=0.01	θ=57.169 d=1.611 SiO2 Irel=0.00	θ =68.801 d=1.363 Si(400) Irel=0.690	θ =69.1388 d=1.36113 Si(400) Irel=100	θ =69.3223 d=1.35444 Si(400) Irel=45.73							
600	θ=10.3253 d=8.56757 ——— Irel=3.72	θ =12.3415 d=7.17207 ——— Irel=73.99	θ=24.937 2 d=3.5707 3 SiB6(150) Irel=57.4 0	θ=29.413 d=3.0367 B(302) Irel=100	θ=37.7549 d=2.38 B(314) Irel=4.90	θ=39.4783 d=2.28204 In(110) Irel=15.62	θ=43.2888 d=2.0911 Si(220) Irel=8.06	θ = 43.8900 d=2.06289 B(330) Irel=4.13	θ=47.5951 d=1.91059 Si(220) Irel=19.43	θ =48.5749 d=1.87452 B(312) Irel=20.4	θ=51.0434 d=1.78802 ——— Irel=2.84	θ =61.2300 d=1.51382 ——— Irel=4.23	θ =68.223 d=1.37444 Si(400) Irel=14	θ =77.1029 d=1.23690 B(550) Irel=2.94						
650	θ=22.6090 d=3.93289 Si(103) Irel=0.69	θ=24.5799 d=3.622 ——— Irel=6.25	θ=29.063 d=3.072 B(314) Irel=13.3	θ=35.753 d=2.512 SiC(111) Irel=1.32	θ=39.175 d=2.2997 In(210) Irel=0.82	θ=42.686 d=2.122 C(100) Irel=1	θ=47.2362 d=1.92427 Si(220) Irel=1.27	θ=68.884 d=1.36198 Si(400) Irel=100	θ=69.882 d=1.36194 Si(400) Irel=43.39										
700	θ=21.584 d=4.1173 SiB4(202) Irel=11.4	θ=24.559 d=3.624 ——— Irel=39.19	θ=28.968 d=3.072 B(314) Irel=100	θ=32.249 d=2.776 In(111) Irel=18.78	θ=35.753 d=2.512 SiC(111) Irel=20.5	θ=38.0030 d=2.36779 ——— Irel=7.1	θ=39.12 d=2.303 In(110) Irel=15.1	θ=40.967 d=2.209 ——— Irel=6.47	θ=43.4015 d=2.101 B(321) Irel=6.98	θ=48.962 d=1.865 C(100) Irel=8.71	θ=49.2305 d=1.8265 Si(220) Irel=4.61	θ=54.0606 d=1.6921 ——— Irel=19.2	θ=60.279 d=1.534 SiC(220) Irel=16.65	θ=60.5199 d=1.5324 SiO2 Irel=0.92	θ=65.165 d=1.4304 ——— Irel=20.64	θ=70.8914 d=1.3283 ——— Irel=18.24	θ=78.7635 d=1.214 SiC Irel=2.6		
750	θ=20.835 d=4.4214 ——— Irel=8.27	θ=24.599 d=3.620 ——— Irel=66.56	θ=29.092 d=3.0606 BQ14 Irel=100	θ=29.970 d=2.9815 SiB6(160) Irel=0.32	θ=34.437 d=2.604 BQ32) Irel=19.43	θ=33.753 d=2.512 SiC(111) Irel=15.3	θ=36.658 d=2.4515 ——— Irel=7.61	θ=39.1225 d=2.3025 In(110) Irel=9.87	θ=42.606 d=2.122 C(100) Irel=12.42	θ =44.526 d=2.03496 C(101) Irel=7.64	θ=46.7783 d=1.9403 ——— Irel=24.53	θ=47.3036 d=1.92545 Si(220) Irel=18.1	θ=48.108 d=1.8865 B(312) Irel=11.75	θ=50.707 d=1.7989 C(102) Irel=32.08	θ=55.325 d=1.6593 B(431) Irel=73.91	θ=67.526 d=1.3863 ——— Irel=47.34	θ=68.307 d=1.3662 Si(400) Irel=47.47	θ=70.0667 d=1.342 ——— Irel=54.56	θ=72.63-15 d=1.30065 SiC(311) Irel=20.42
800	θ=22.2365 d=3.996 ——— Irel=6.87	θ=24.316 d=3.6100 ——— Irel=66.62	θ=27.883 d=3.1996 5 ——— Irel=5.15	θ=29.066 d=3.0722 B(214) Irel=100	θ=31.317 d=2.856 B(233) Irel=5.5	θ=33.7016 d=2.3349 SiC(011) Irel=15.9	θ=39.054 d=2.3045 In(110) Irel=9.19	θ=40.5667 d=2.2344 Irel=19.6	θ=42.6 d=2.122 C(100) Irel=	θ =47.265 d=1.923 Si(220) Irel=11.0	θ=56.4020 d=1.631 Si(311) Irel=3.91	θ=60.7914 d=1.5237 Irel=4.49	θ=64.4952 d=1.445 ——— Irel=6.55	θ=69.0171 d=1.3597 Si(400 Irel=35.27					

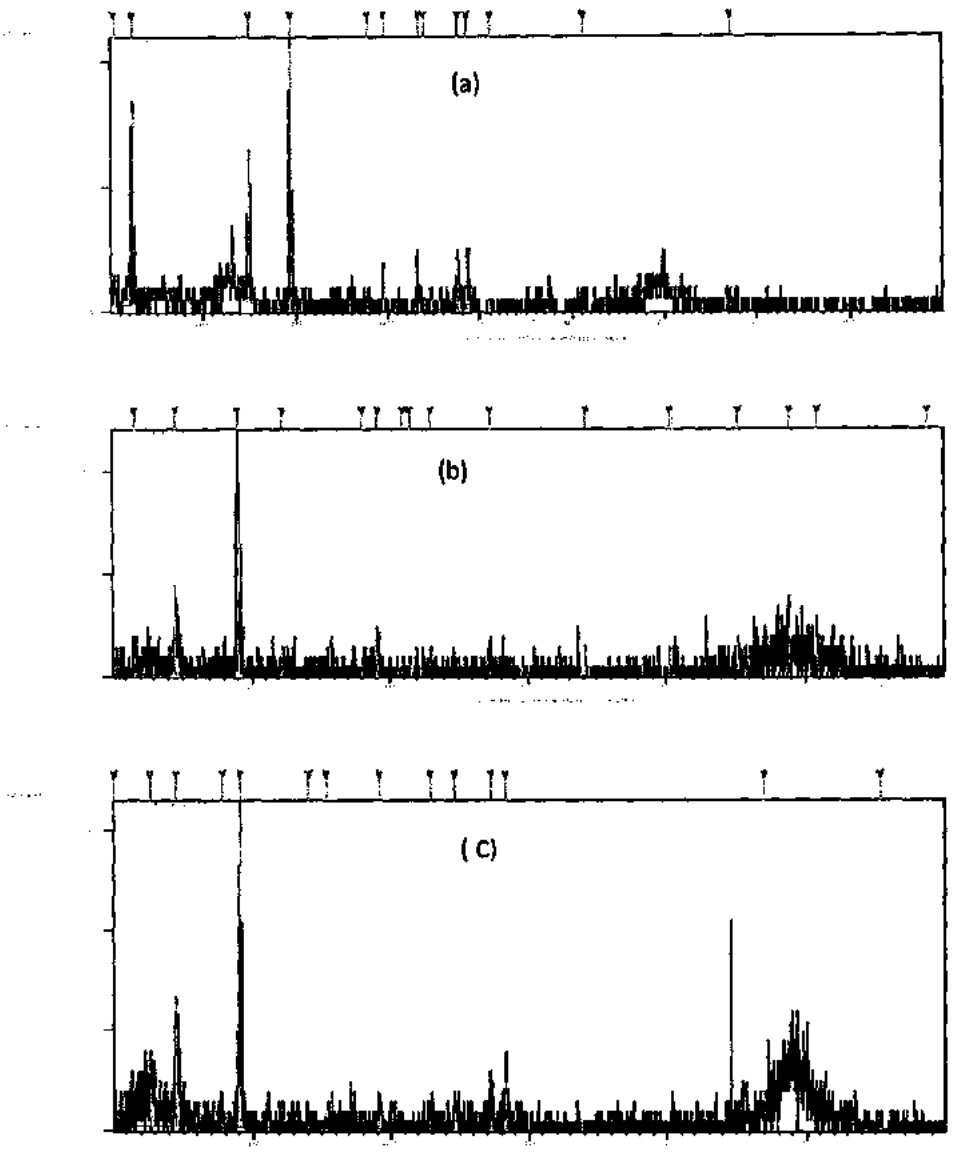


Figure 5.43: (a) XRD machine as obtained for In+C co implanted n-type silicon substrate for (a) as-implanted (b) RTA post-annealed at 600°C. (c) RTA post-annealed at 700°C.

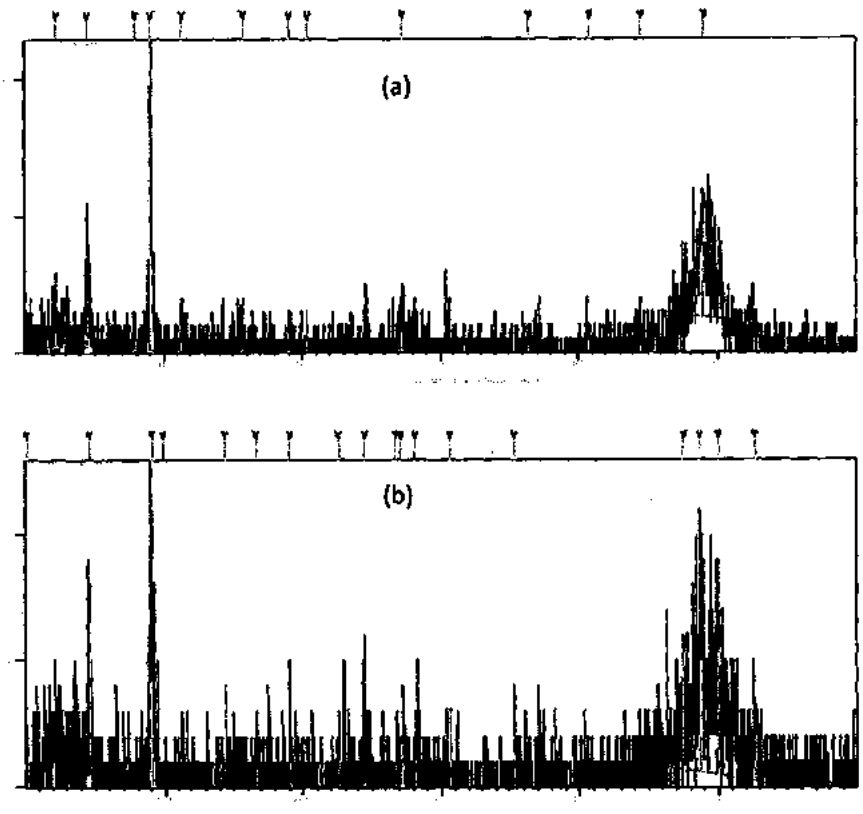


Figure 5.43: XRD as obtained from machine for In+C co-implanted n-type silicon substrate for (a) RTA post-annealed at 750°C. (b) RTA post-annealed at 800°C.

5.6 Analysis of Grazing Incidence X-Ray Flouresence Measurements

Grazing incidence X-Ray flourescence (GIXRF) analysis in the soft X-Ray range is a high potential tool for obtaining information about the implantation profile because in depth changes of the X-Ray Standing Wave (XSW) intensity are dependent on the angle of incidence [64]. Since the dopant atoms in ultra shallow junctions are mostly confined to the first few nanometers, grazing incidence X-ray fluorescence (GIXRF), whose probing depths are around 10 nm, is applied to evaluate the retained dose and possibly the depth distribution of the dopants. Keeping this very fact, in mind we have tested our samples against GIXRF protocols. In this technique the reflectance of the sample is measured as a function of grazing incidence angle of X-rays.

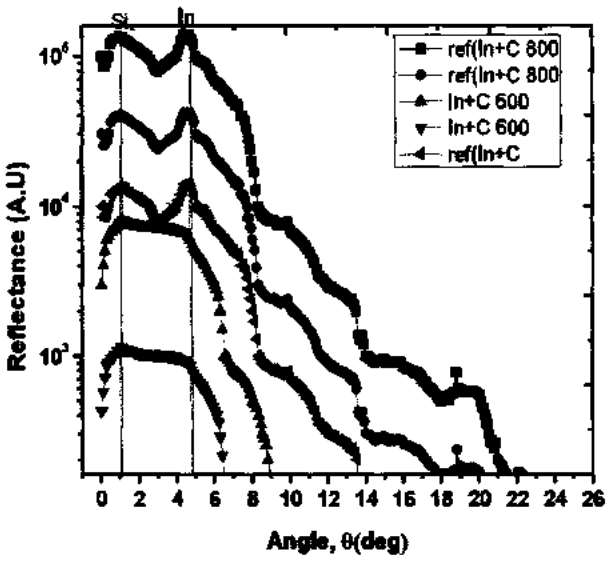


Figure 5.44: This graph shows the experimental GIXRF data and the calculated angular dependence of the fluorescence intensity for the In+C co-implanted silicon substrate.

Figure 5.44 shows the experimental data and the calculated angular dependence of the fluorescence intensity for the In+C junctions in n-type Si devices. These experimental X-Ray reflectivity curves were recorded for In+C at film thickness annealed at different temperatures. It also shows that by increasing angle, X-ray flourescnce intensity decreases but this trend changes after 1.1 degree which is the critical angle for silicon, the reflectance decreases. It is obvious that the shape of the profile for cases annealed at 600°C is different from the ones annealed at 800°C and as-implanted samples. The maximum of the profiles for as-implanted and 800°C annealed samples are located at the critical angle of Indium (4.85 degree for 0.28 keV and 0.29 keV excitation energy) whereas the maximum of the profiles for the samples annealed at 600°C are located at the critical angle of silicon (1.1 degree for 0.28 keV and 0.29 keV excitation energy). For getting scans of higher angular resolution at the critical angle of total reflection, variable step size was used. Some degrees below and above the critical angle the angular increment was increased. For all as-implanted and annealed samples, as the profile tends toward a constant value, the intensity differences in that region gets smaller as shown in figure 5.44. Values at angles far above the critical

angle are independent of the profile shape and provide an estimate of the total implanted dose.

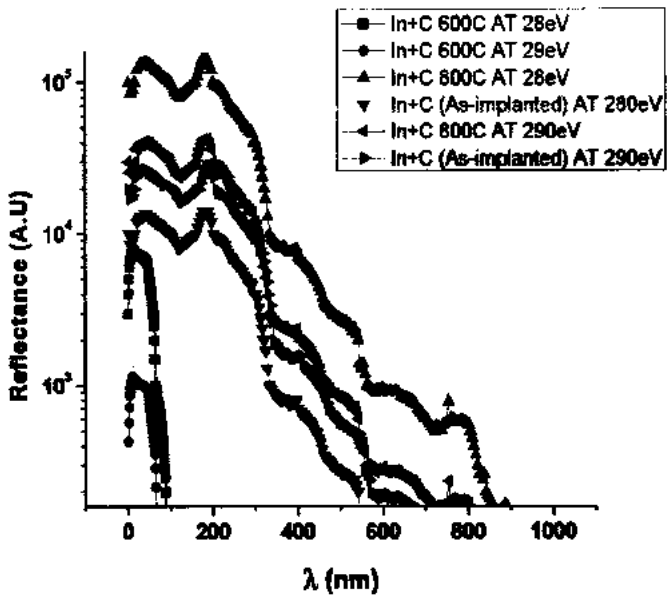


Figure 5.45: The experimental GIXRF data shows the fluorescence intensity of In+C co-implanted silicon samples (both as-implanted and annealed) with respect to wavelength.

In order to find the offset in the angle, the divergence of the beam and a flux/geometry factor, this Si (bulk/substrate) curve is used to fit the data. These parameters are subsequently used for processing and fitting of the In+C angular curve. The divergence value is used as initial estimate of the divergence in the In+C fit, the angle offset is used to correct the angular scale of the In+C intensity curve, and the geometry factor is used as a scaling factor.

As it is known that atoms in ultra-shallow junctions are mostly confined near the surface with-in depth of few nanometers, the variation of the flourescence signal as function of of the incidence angle gives indication on the depth distribution of the excited species by interference effects of radiation reflected from the layer surface and radiation reflected from the layer/substrate interface [142,143]. The sampling depth can be varried by changing the x-ray beam incidence angle from zero up to couple of times

the critical angle for total reflection. Because X-rays from thin films shows the oscillation known as the Kiessig fringes, which provide information on the layers. The oscillation intervals which come from the interference of X-rays at a thin film, is approximated by $\theta=\lambda/t$, where, θ is the glancing angle of an X-ray, λ, is the wavelength of an X-ray and t, is the layer thickness. It shows that the interference interval increases with the decrease of layer thickness as shown in figure 5.45. The measured junction depth for samples annealed at 600°C is 9 nm, for samples annealed at 800°C is 39 nm and 40 nm for as implanted samples. In fact, the resulting In+C distributions have shallower projected ranges, Rp for samples annealed at 600°C, than the others expected from RBS and Ellipsometry. This also shows almost same projected range for samples annealed at temperature greater than 600°C.

5.7 Roughness Measurements by AFM

One of the most critical steps for the fabrication of ultra shallow junction is the study of surface morphology. At present, the most promising approach to fulfill this goal is atomic force microscopy system, which has been opportunely modified in order to perform surface morphology. Figures 5.46-5.50 demonstrate the topographical view of the In+C co-implanted Si Substrate before and after annealing showing extent of roughness and uniformity of the deposited Indium and Carbon co-implants. The presence of impurity concentration of boron at different depths is also visible as background structural information. These three dimensional views show negligible degradation of the morphology of the surface after the devised and processed implant strategy. Positioning of thermal flux to the annealing effects considerably reduces damages and is crucial to study the consequent damage re-engineering in Si-based CMOS devices and thus we analyze the devices again after undergoing the annealing of fabricated devices in the formation of effective depth of ultra-shallow junction. Figure 5.51 shows the variation of RMS, as a function of temperature, which shows that the surface roughness increases with increasing temperature. Root mean square (RMS or Rq) is the square root of the arithmetic mean of the square of the vertical deviations from the reference- line. An output measurement parameter RMS is connected with the distribution's probability density function, and serve as a quick

evaluation tool to analyze the pre and post processed surface morphology. The values reported are average of six measurements at different locations of the samples. These results are consistent with previously reported studies.

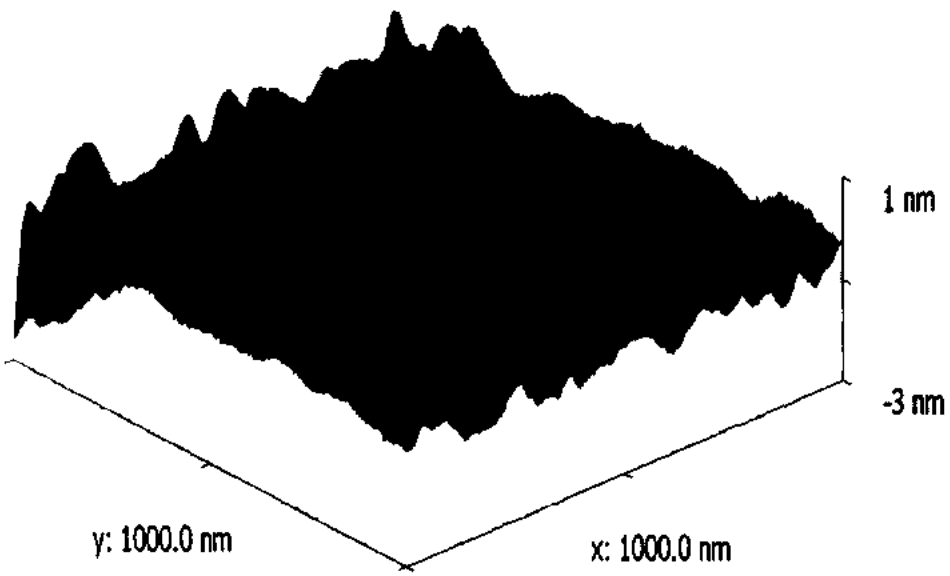


Figure 5.46: Atomic Force Microscopic topographical view of the In+C co-implanted Si Substrate before annealing showing extent of roughness and uniformity of the deposited indium and carbon co-implants. This three dimensional view shows negligible degradation of the morphology of the surface after the devised and processed implant strategy for effective utilization in the formation and integration of CMOS ultra- shallow junction.

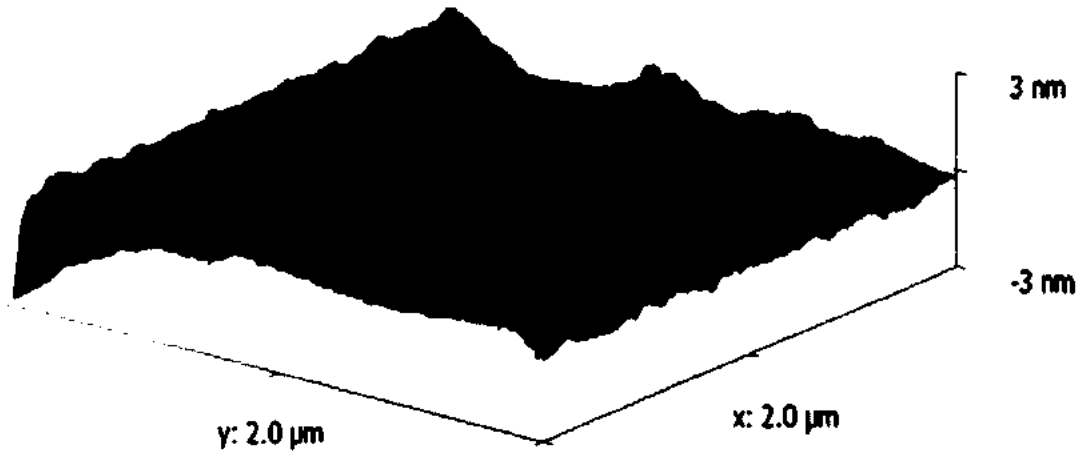


Figure 5.47: Atomic Force Microscopic topographical view of the In+C co-implanted Si Substrate RTA annealed at 600°C showing extent of roughness and uniformity of the deposited indium and carbon co-implants.

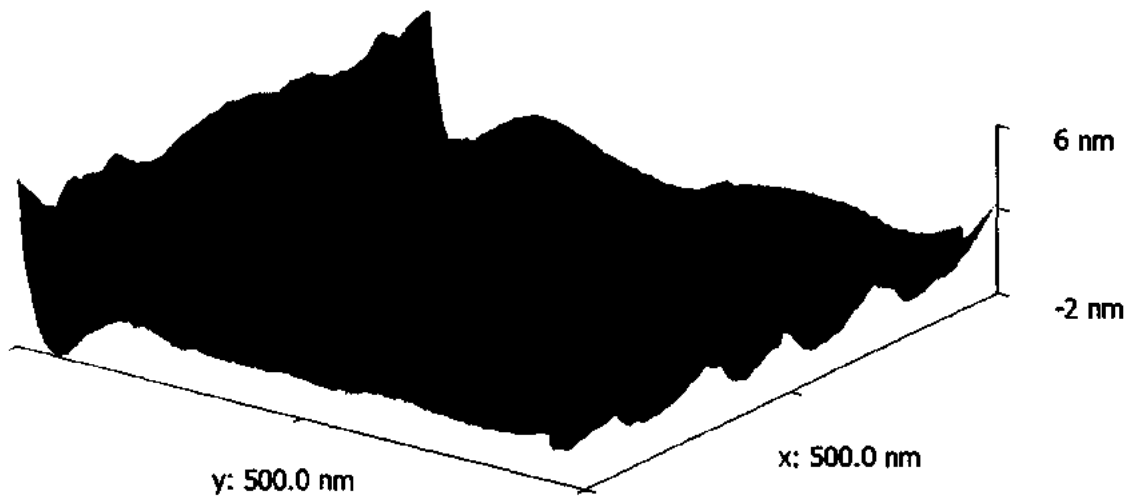


Figure 5.48: Atomic Force Microscopic topographical view of the In+C co-implanted Si Substrate RTA annealed at 700°C showing extent of roughness and uniformity of the deposited indium and carbon co-implants.

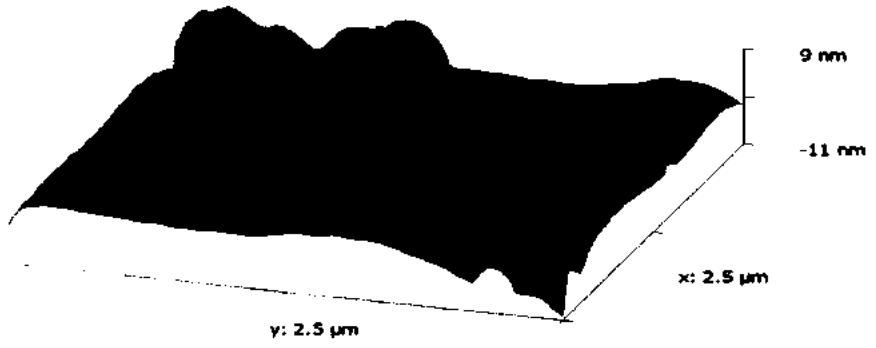


Figure 5.49: Atomic Force Microscopic topographical view of the In+C co-implanted Si Substrate RTA annealed at 750°C showing extent of roughness and uniformity of the deposited indium and carbon co-implants.

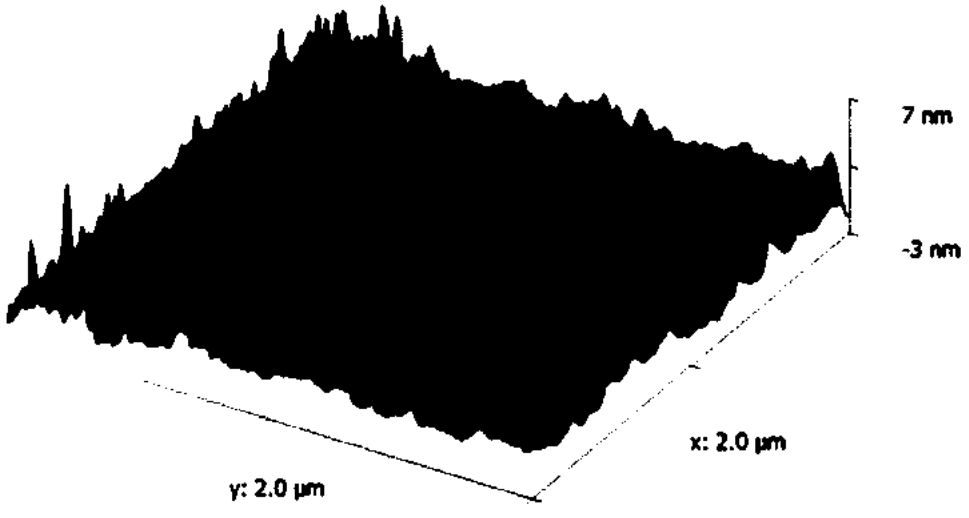


Figure 5.50: Atomic Force Microscopic topographical view of the In+C co-implanted Si Substrate RTA annealed at 800°C showing extent of roughness and uniformity of the deposited indium and carbon co-implants.

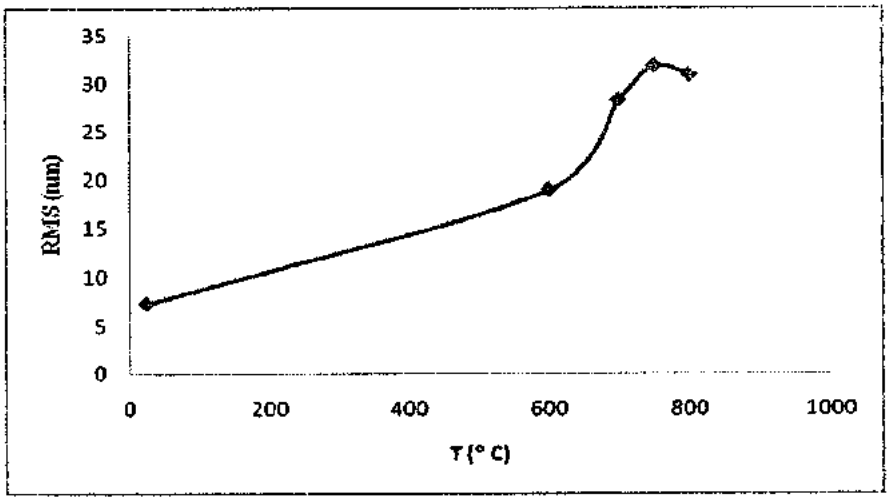


Figure 5.51: Variation of surface roughness amplitude parameters as a function of annealing temperature for In+C co-implanted Si-substrates.

5.8 Discussion and Analysis of B implanted N-Type Silicon

The industry standard technique for junction formation is low energy ion implantation followed by a spike anneal. During the spike anneal, significant diffusion, boron clustering, and defect evolution occurs which result in deeper junctions and increased sheet resistance [144, 145, 146]. The conventional methods are prone to broaden the dopant profile due to the interaction between implantation induced defects (point defects, TED) [147, 148].

This part of the work focuses to optimize processes window for n-type B^+ implanted silicon by calculating sheet resistance, sheet carrier concentrations, mobility and junction depth with various implantation and annealing conditions. In order to lower the sheet resistance of n-type B^+ implanted silicon, samples were processed with two different annealing techniques, performed at operational window from 600-1100°C. The primary aim is to fabricate USJs for the process optimization application in nano CMOS devices through the understanding and maneuvering of dopant interactions with substrate.

In order to find out the resultant range and damage profile in the Si due to ions, rigorous simulations were performed with various ion energies at different incident angles' using computer code Stopping and Range of Ions in Matter [7]. These simulations constitute the central part of the experiment because very careful parameter optimization is required to study the process sequence to fabricate ultra-shallow junctions. These simulations are also very important to compare the characterization data with the simulated ones in order to generate a workable model for actual devices. The results of the SRIM (Stopping and Range of Ions in Matter) simulations selected for the fabrication of the device are shown in figure 5.52. This figure exhibits carefully simulated positions of the 30 keV boron implanted n-type Si. The peak concentration of 9.95×10^{19} atoms/cm^3 appears at the depth of 67 nm in silicon. These experimental results show that junction formation occurs near about simulated junction depth. The position of the junction, for as implanted is at 70 nm and vary from 35 nm to 89 nm by varying annealing temperature. Figure 5.53 shows the defect generated due to boron ion implantation in n-type silicon.

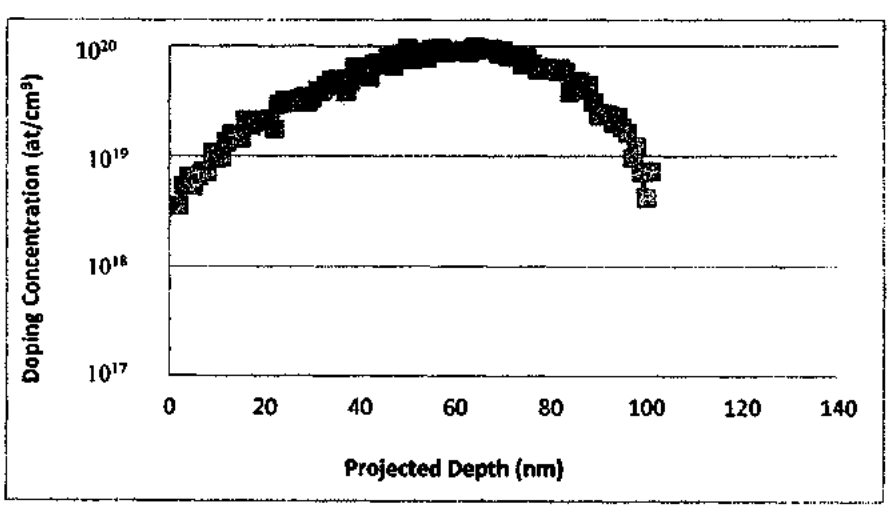


Figure 5.52: Simulated positions of the 30keV boron implanted n-type silicon. Simulations carried out by computer code SRIM.

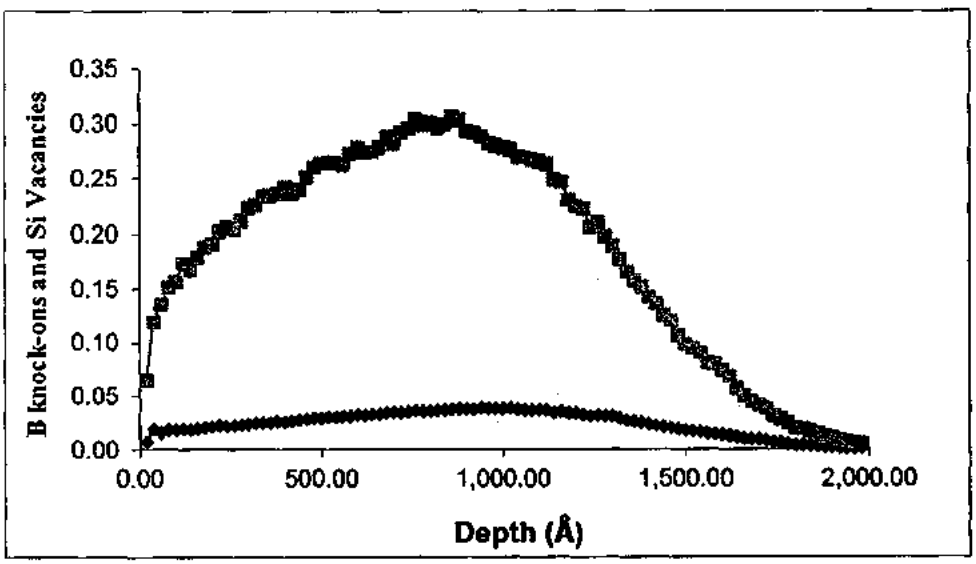


Figure 5.53: TRIM simulation results showing defects generated due to implantation of boron (30 keV energy) in n-type Si-substrate. The high end defect profile exists outside the area of interest.

For finding the junction optimization, the junction thermal stability evaluated based on de/re-activation studies were performed by RTA annealing in the temperature range from 600°C to 800°C for 60 sec and furnace annealed at 1050°C for 15 min. The obtained data were plotted in terms of R_s values versus the temperature as shown in above figures. 5.54-5.57. It is evident that sheet-resistance of the implanted samples vary as a function of annealing temperature, again with the averaged values of repeated measurements in each case.

The results show that the junctions post annealed at 600°C have sheet resistance lower than those at 650°C, but after 650°C reductions in sheet carrier concentration and increase in sheet resistance is observed. This suppression of sheet resistance is due to a reduction in the deactivation of the carrier concentration and improved mobility as shown in figure 5.63. We can also describe this phenomena in this way that a high level of B atoms activation is achieved at 600°C. But after increasing the temperature amorphous layer of boron re-crystallized. Near the surface at high boron concentration region boron interstitial nucleation occurs resulting in the increasing in sheet resistance

and mobility and decrease of sheet carrier concentration as shown in figures 5.54, 5.55 and 5.62. Figures 5.54 and 5.55 also shows that at 600°C due to deactivation sheet carrier concentration is high but after increasing temperature from 600°C -650°C reduction in deactivation causes suppression of sheet carrier concentration. Figures 5.56, 5.57 and 5.58 are providing a process window of sheet resistance for optimization processes by providing variation of sheet resistance with respect to current range from 1nA to 35 nA at different annealing temperatures.

In summary, from these results it has been concluded that the electrically active dose, as well as the sheet carrier concentration, increase with increasing temperature. At the same time, the junction depth is only weakly increased as shown in Table 5.3. All of this would suggest that mobility decreases, but the mobility was also found to increase after increasing temperature from 600°C as shown in figure 5.62. Therefore it can be concluded that the quality of the crystal improved. For the sample with an elevated temperature from 700°C-800°C, the sheet resistance and mobility increase on the one hand and the sheet carrier concentration decrease on the other hand. In this case the mobility increase is likely due to a reduction of the electrically active dose as is also seen in the sheet resistance.

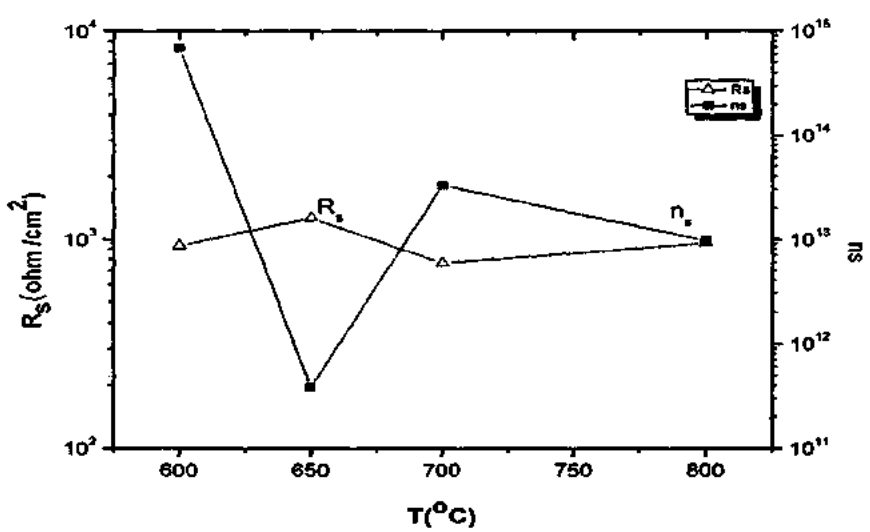


Figure 5.54: Effect of annealing g temperature on Sheet resistance and sheet carrier concentration for the 30 keV boron implanted n-type silicon (S#1).

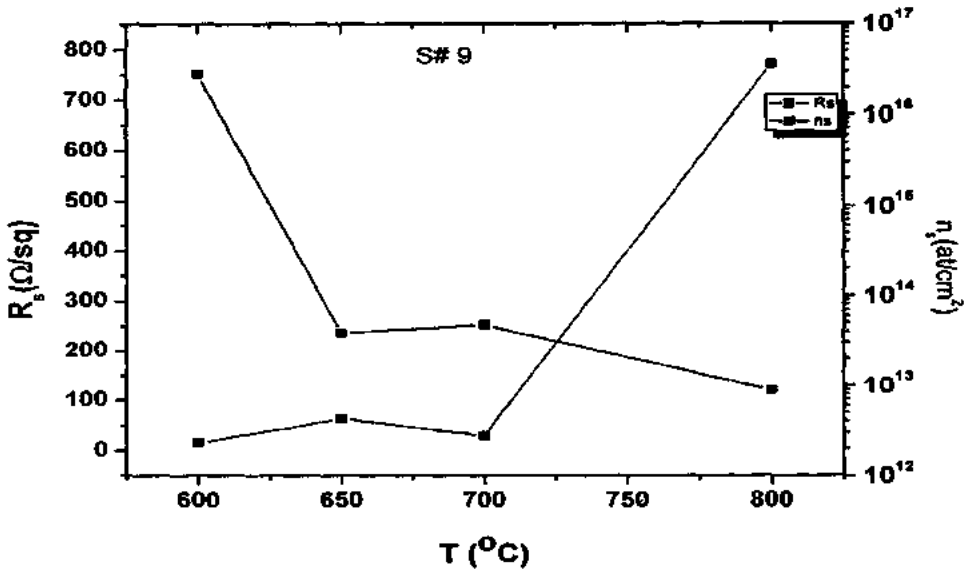


Figure 5.55: Effect of annealing g temperature on sheet resistance and sheet carrier concentration for the 30 keV boron implanted n-type silicon (S#9).

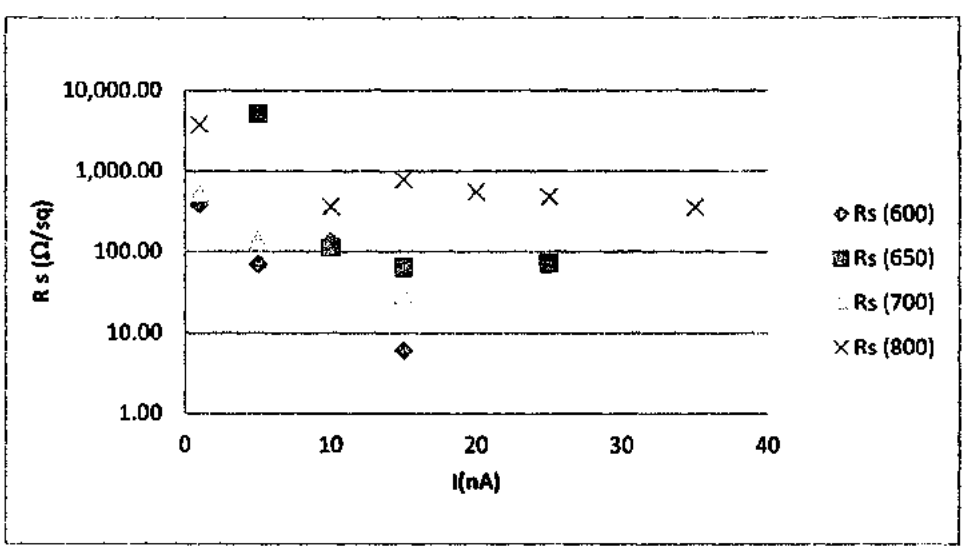


Figure 5.56: Effect of applied current on sheet resistance of 30 keV B implanted n-type silicon annealed between temperature regime 600°C-800°C.

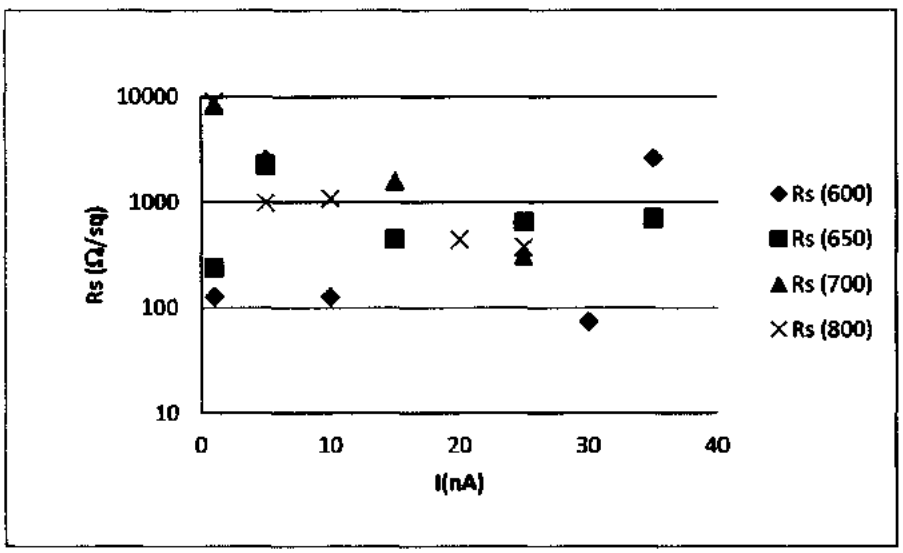


Figure 5.57: Effect of applied current on sheet carrier concentration of 30 keV B implanted n-type silicon (sample#1) annealed between temperature regime 600°C-800°C.

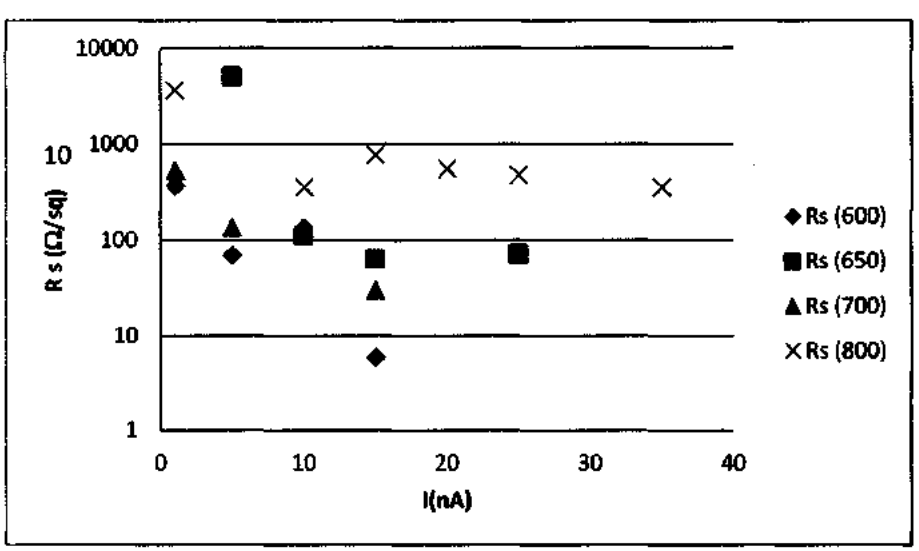


Figure 5.58: Effect of applied current on sheet resistance of 30 keV B implanted n-type silicon (sample#9) annealed between temperature regime 600°C-800°C.

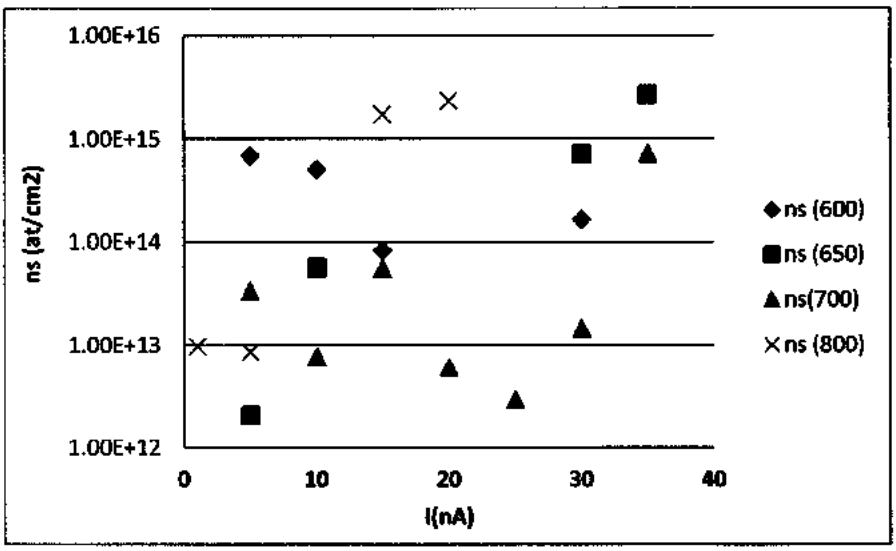


Figure 5.59: Effect of applied current on sheet carrier concentration for 30 keV B implanted n-type silicon (sample#14) annealed between temperature regime 600°C-800°C.

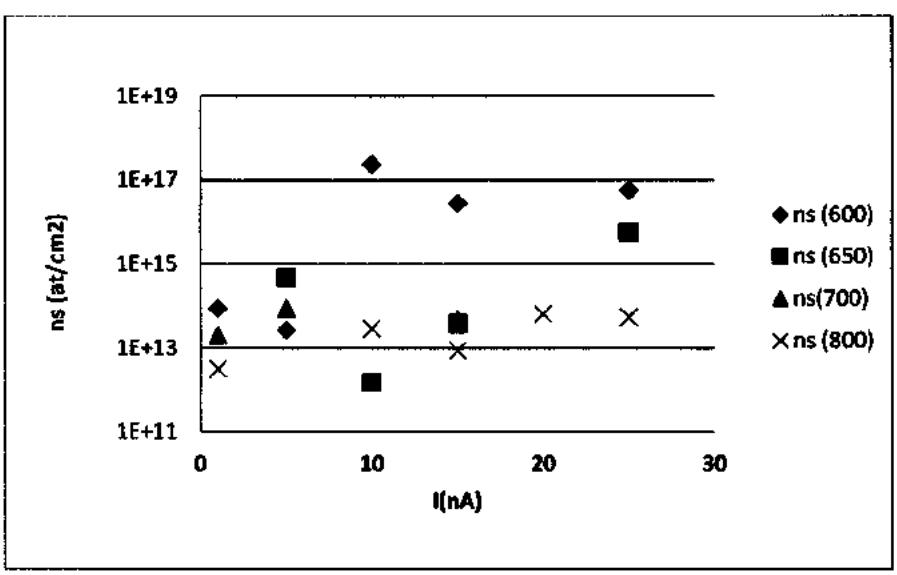


Figure 5.60: Effect of applied current on sheet carrier concentration for 30 keV B implanted n-type silicon (sample#9) annealed between temperature regime 600°C-800°C.

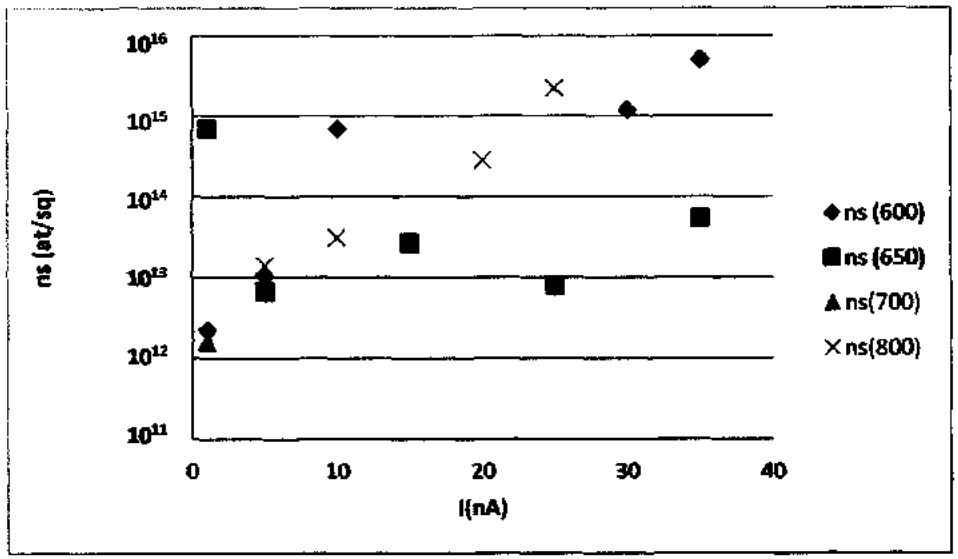


Figure 5.61: Effect of applied current on sheet carrier concentration for 30 keV B implanted n-type *ad* (sample#1) annealed between temperature regime 600°C-800°C.

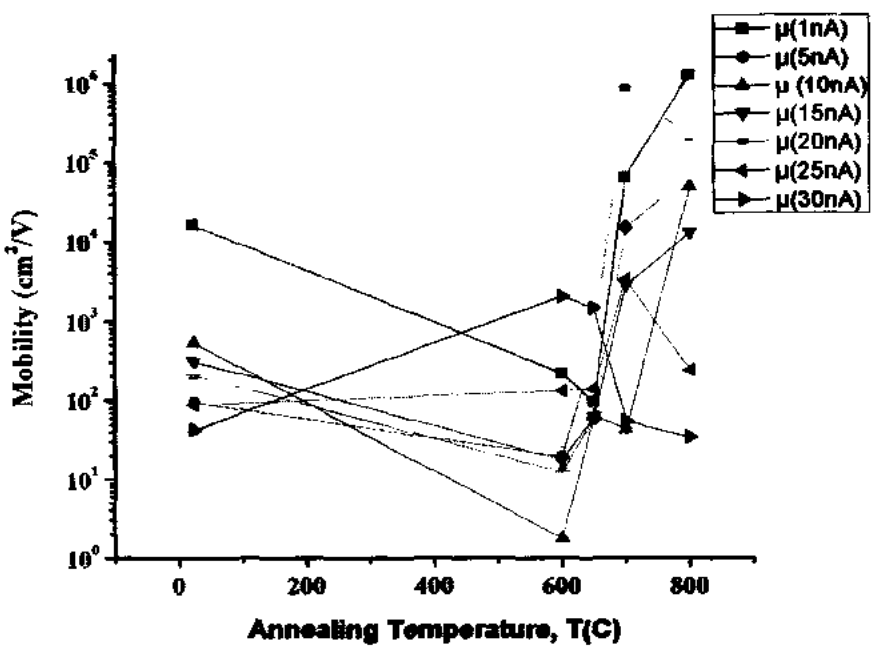


Figure 5.62: Effect of applied current on mobility for 30 keV B implanted n-type silicon (sample#1) annealed between temperature regime 600°C-800°C.

Table 5.3: Data table of junction depths obtained from CV measurement system.

Sample. No.	ion on implantation energy (keV)	Annealing Temperature (°C)	Junction Depth (nm) at R_p of the distribution
1	30	As-implanted	70
2	30	As-implanted	69
3	30	As-implanted	70
4	30	As-implanted	69
5	30	As-implanted	69
6	30	As-implanted	88
7	30	As-implanted	74
8	30	As-implanted	89
9	30	As-implanted	89
10	30	As-implanted	70
11	30	As-implanted	69
12	30	As-implanted	70
13	30	As-implanted	81
14	30	As-implanted	39
15	30	As-implanted	65
16	30	As-implanted	89
17	30	As-implanted	40
18	30	As-implanted	69
19	30	As-implanted	70
20	S#1	600/60sec RTA	66
21	S#1	700/60sec RTA	69
22	S#1	750/60sec RTA	70
23	S#1	800/60sec RTA	69
24	S#1	1050/15min Furnace annealed	75
25	S#9	600/60sec RTA	80
26	S#9	700/60sec RTA	85
27	S#9	750/60sec RTA	89
28	S#9	800/60sec RTA	88
29	S#9	1050/15min Furnace annealed	90
30	S#14	600/60sec RTA	35
31	S#14	700/60sec RTA	39
32	S#14	750/60sec RTA	38
33	S#14	800/60sec RTA	43
34	S#14	1050/15min Furnace annealed	55

Rutherford Backscattering (RBS) measurements were used to determine the boron implantation profile depths by using a 2.085 MeV He^+ ion beam backscattered at an angle θ of 170° from silicon target on which boron, oxygen and phosphorous are present as surface impurities as shown in figures 5.64-5.68. The oxygen impurity is due to the self oxidation on the surface and phosphorus traces are due to n-type initial material.

In figures 5.63, 5.64, 5.65 and 5.66, the RBS of the as-implanted and as-annealed specimens of 30 keV B implanted n-type silicon are shown with those of the random and aligned specimens. This shows that the RBS spectrum of as-implanted 30 keV B^+ implanted samples does not reveal significant damage, and the RBS/C spectrum of the as annealed one is almost identical to that of the aligned specimen. The backscattered energy and concentration of impurity atoms calculated from figures 5.64-5.68 is shown in Table 5.4. Figure 5.63 shows that the silicon substrate returns a thick target whose leading edge is at channel number 610 with backscattered energy of 1.28 MeV and backscattered energy for boron is 0.45 MeV (channel number 200). Figure 5.64 shows silicon surface corresponds to a backscattered energy of 1.2 MeV at channel number 580 and backscattered energy for boron is 0.48 MeV at channel number 200.

The residual damage of the as implanted 30 keV B^+ is slightly larger than that of the annealed B^+ implanted silicon (after 15 min of furnace annealing at 1050°C and 600°C/60 sec, 700°C/60 sec RTA anneal). This process is due to the presence of an excess Si interstitials near the neutral region, which is used to fill or repair the nearby vacancies during annealing. The plateau shape of the backscattered yield in figure 5.68 at channel number 200 demonstrates that the layer tend to go amorphous.

Table 5.4: Concentration and back scattered energy of impurity atoms (B) in 30keV boron implanted n-type Silicon.

Sample I.D	Backscattered Energy (MeV)	Conc (at/cm^3)
30keV n-type B-implanted(S#1)	0.12	2.48×10^{18}
30keV n-type B-implanted(S#14)	0.48	2.54×10^{18}
30keV n-type B-implanted(S#9)	0.16	2.42×10^{18}
30keV n-type B-implanted (annealed#1050°C)	0.15	2.33×10^{18}
30keV n-type B-implanted Anneal#600°C	0.14	2.28×10^{18}
30keV n-type B-implanted Annealed#700°C	0.141	2.24×10^{18}

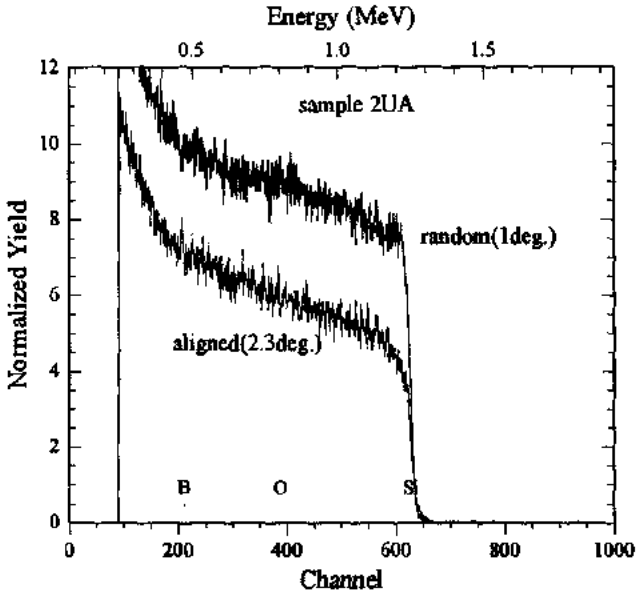


Figure 5.63: RBS channeling spectra of born implanted n-type silicon with a dose of 1×10^{15} at/cm^2 and energy 30 keV (sample#2 as-implanted). The samples are aligned with the (100) channel.

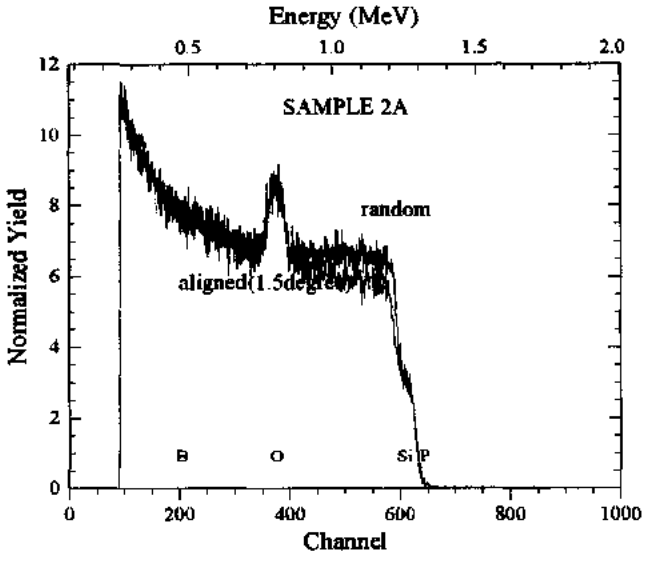


Figure 5.64: RBS spectra n-type silicon implanted with a born dose of 1×10^{15} at/cm^2 and energy 30 keV and annealed at 1050°C (sample#2). The samples are aligned with the (100) channel

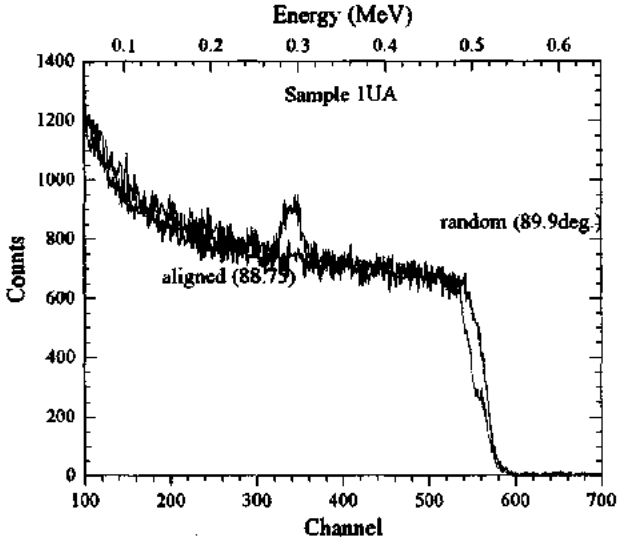


Figure 5.65: RBS spectra n-type silicon implanted with a born dose of 1×10^{15} at/cm^2 and energy 30 keV (sample#1 as-implanted). The samples are aligned with the (100) channel.

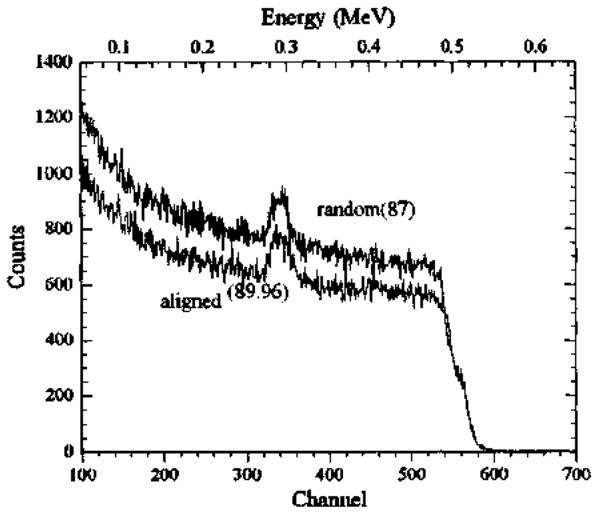


Figure 5.66: RBS spectra n-type silicon as- implanted with a born dose of 1×10^{15} at/cm^2 and energy 30 keV and annealed at 1050°C (sample#1). The samples are aligned with the (100) channel.

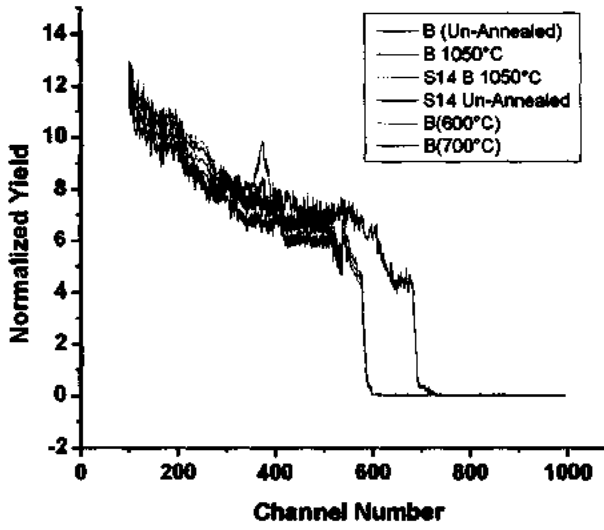


Figure 5.67: Comparative normalized yield spectra for n-type silicon implanted with a born dose of 1×10^{15} at/cm^2 and energy 30 keV for both as-implanted and annealed samples. The samples are aligned with the (100) channel.

Chapter No. 6

6.1 Conclusions

1. The formation of stable abrupt ultra shallow junction with suppressed sheet resistance at different annealing temperatures has been achieved by using low thermal budget RTA.

2. The junction remains stable undergoing post implant thermal cycles between 600-800^{0}C while achieving the depths between 9 nm to 60 nm. The quality, shape and profile of the ultra shallow junction as exhibited by electro-optical parameters in this study have ramifications for device engineers while fabricating CMOS on sub 10 nm technology nodes

3. It was also concluded that conduction near the surface is due to interstitials, so we need less energy (172 meV) to activate indium and carbon atom by applying lower thermal budget.

4. By applying different current ranges (1nA-30 nA) a window of controlled values of sheet resistance, sheet carrier concentration and carrier mobility is provided, which will help us in increasing the device performance and controllability.

5. The thermal effects on structural and morphological properties of the layers engineered by co-implantation technology in Si provides a controlled, reliable, repeatable and easy to drive process directly impacting the physical activity at atomistic level (defect clustering, movement of dopant atoms within the atomic distribution profiles, surface roughness, lattice relaxation and strain) to fabricate ultra-thin piezoresistors and ultra shallow junction for CMOS compatible fully integrated systems.

6. In short this study provides a reasonable scientific contribution to the understanding of the formation of ultra shallow junctions and optimization processes because the formation of USJs is investigated through a systematic study by Rapid Thermal Annealing (RTA). Results obtained through different techniques were according to the order of the requirements for sub-45 nm CMOS generations, RTA is also a promising technique for shorter annealing time (to limit dopant diffusion) and higher peak temperature (to maximize dopant activation). Sub-15 nm junctions with lower sheet resistance (250-1000 ohm/squ) were achieved with annealing, meeting the specifications for 32 nm CMOS technology node.

6.2 Recommendations for Future Work

Although several new findings and improvements to the existing knowledge base have been achieved on the new USJ formation techniques during the course of this work, there are certainly some areas and details where required to be done in order to acquire further understanding on the advanced USJ technology. This selection outlines some of the possible avenues that could be followed on from this work:

- From the evaluation discussed in chapter 4, Secondary Ion Mass Spectroscopy (SIMS) may be utilized as an alternative of measuring and monitoring thickness of ultra shallow junctions in In+C co-implanted silicon substrate and boron implanted n/p type silicon substrate.
- The thermal budget experiments can be further studied by using other annealing techniques like laser annealing by varying the substrate temperature. Since the cooling rate of the LTP is controlled by the temperature difference between the surface and the substrate, because a higher substrate temperature would result in a lower cooling rate, which is used to reduce the thermal stress induced in the substrate. It is also possible to use complex schemes such as multiple laser pulses with varying fluencies in all such experiments
- It can be further studied by using He ion beam and H ion beam of various energies at different incident angles. By doing this we can find the exact location of dopants.
- The electrically active ultra shallow junction can also be studied by using advanced techniques such as scanning capacitance microscopy (SCM). The lateral distribution of dopants in semiconductor devices has an increasing effect on the device characteristics. As the critical dimension decreases. So it becomes necessary to find the two-dimensional (2-D) dopant profiles of actual devices. Contrary to the SIMS technique SCM has been developed to give a more accurate analysis on 2-D dopant distribution. .

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